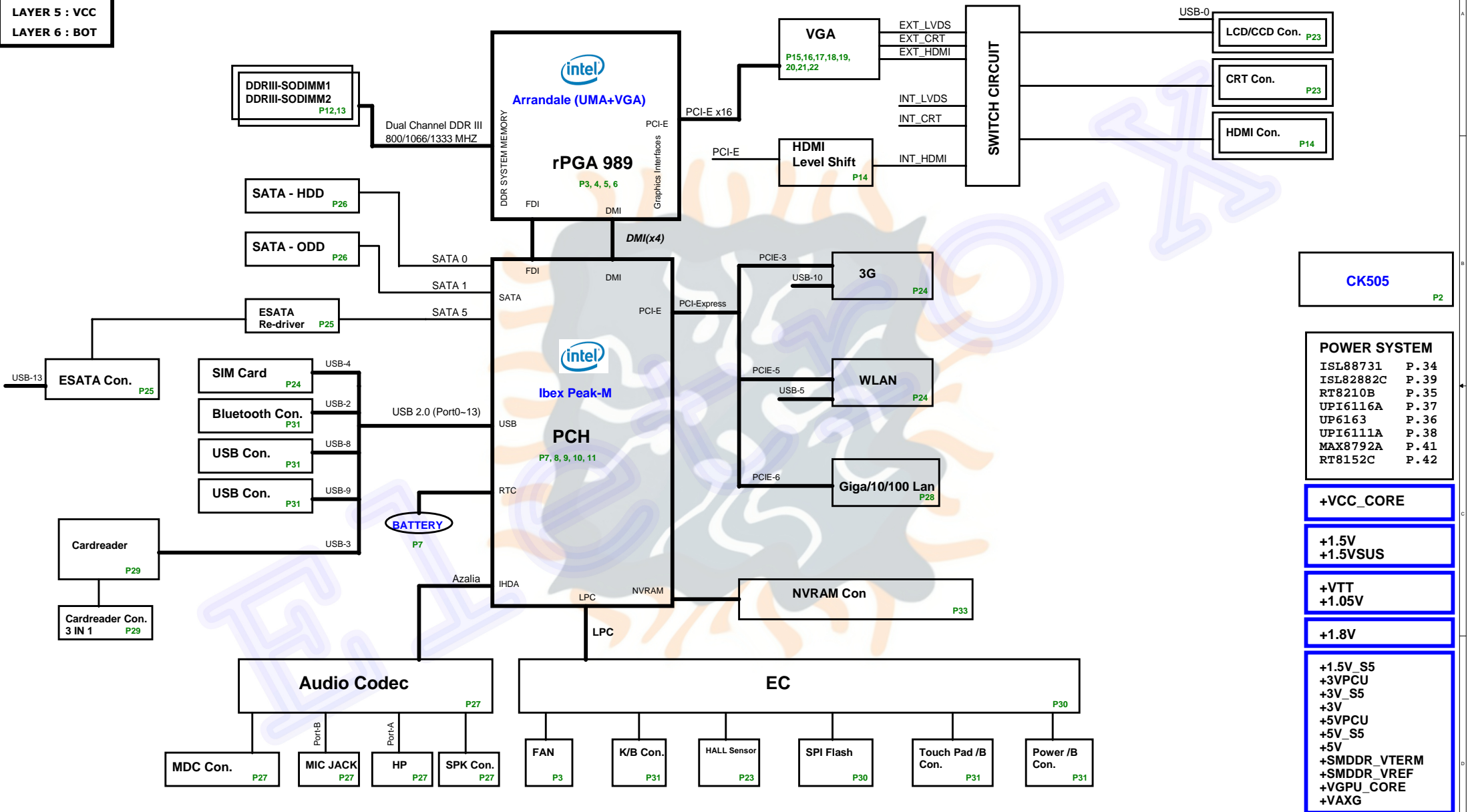


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

BL6 Block Diagram

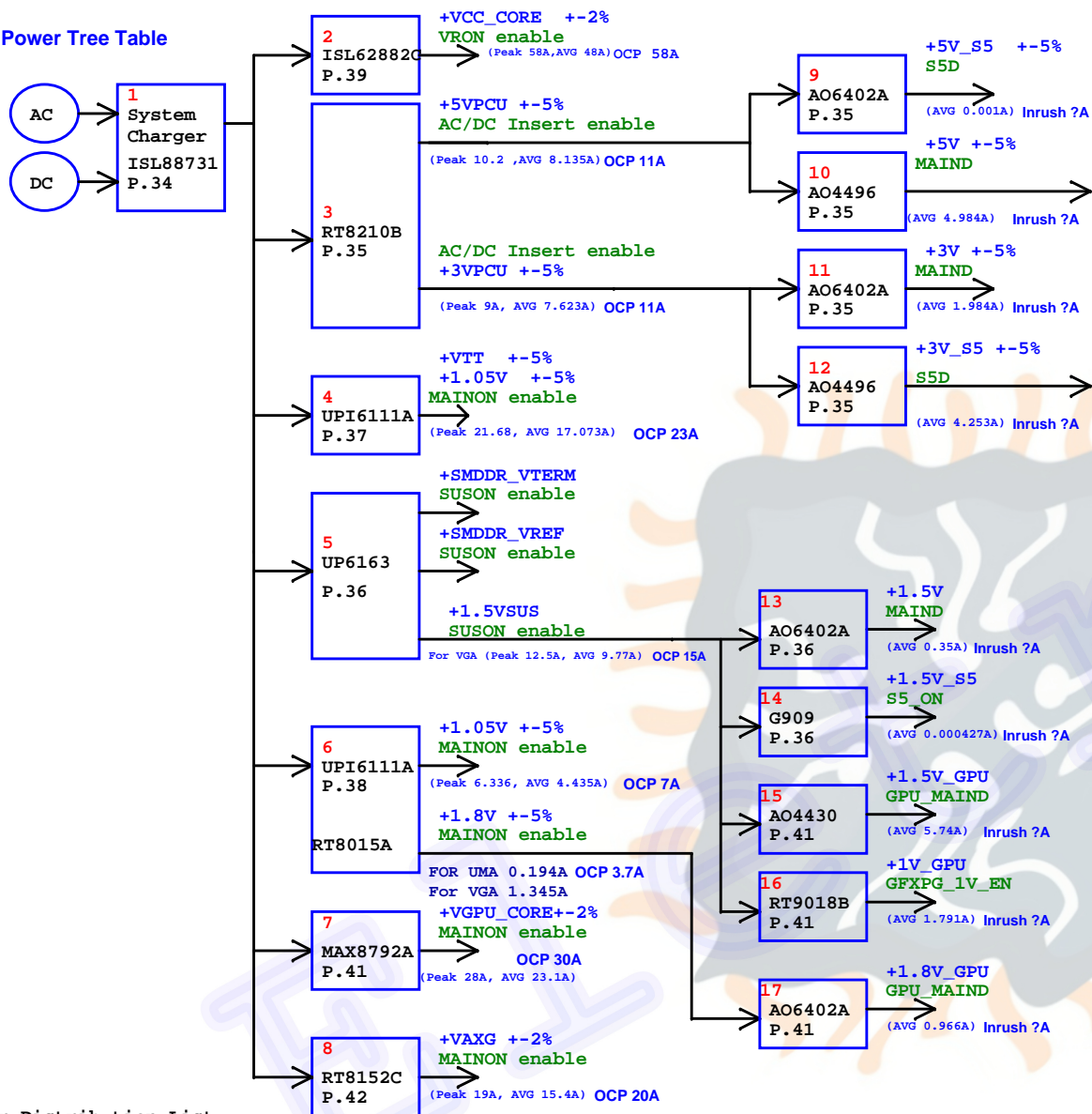


POWER SYSTEM

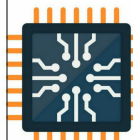
ISL88731	P. 34
ISL82882C	P. 39
RT8210B	P. 35
UPI6116A	P. 37
UP6163	P. 36
UPI6111A	P. 38
MAX8792A	P. 41
RT8152C	P. 42

- +VCC_CORE
- +1.5V
- +1.5VSUS
- +VTT
- +1.05V
- +1.8V
- +1.5V_S5
- +3VPCU
- +3V_S5
- +3V
- +5VPCU
- +5V_S5
- +5V
- +SMDDR_VTERM
- +SMDDR_VREF
- +VGPU_CORE
- +VAXG

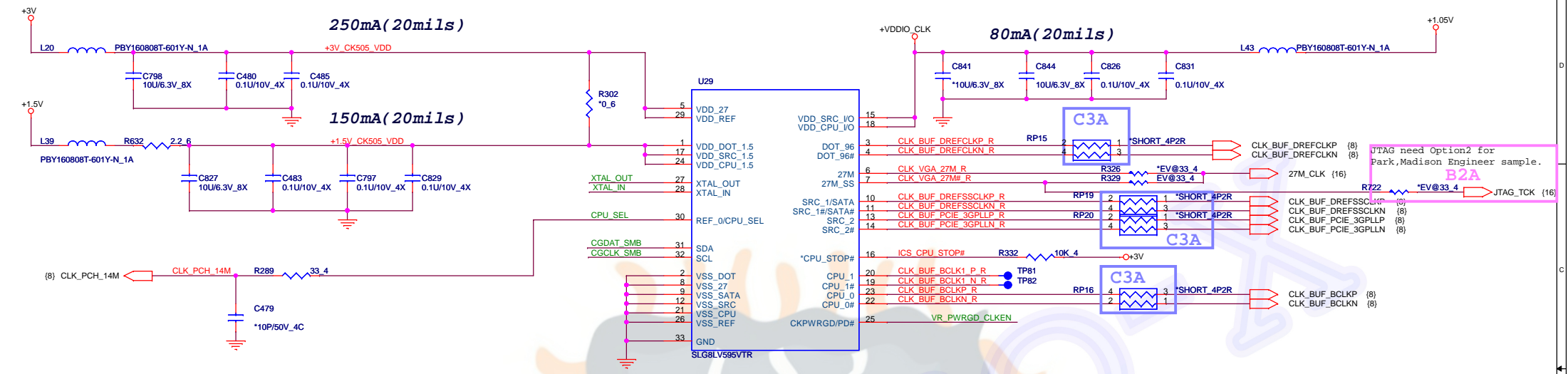
Power Tree Table



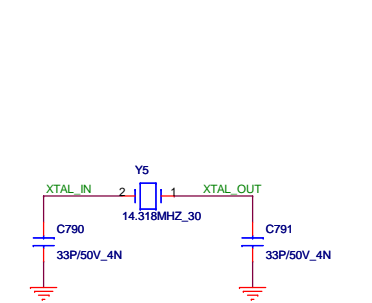
Power Distribution List

[illegible]

CLOCK Gen



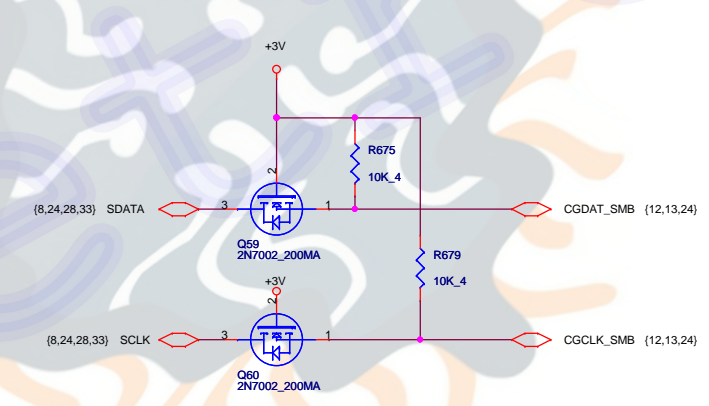
CLK CRYSTAL



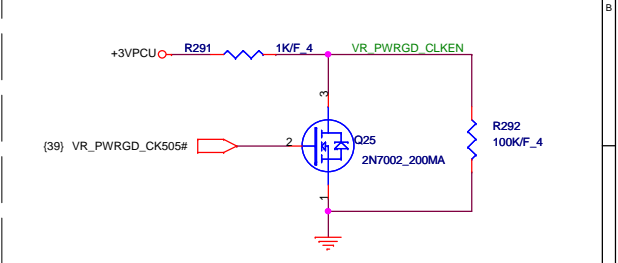
CLK CPU_SEL

	0	1
CPU_SEL	CPU =133MHz	CPU=100MHz
	(default)	

CLK I2C

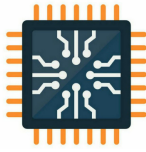


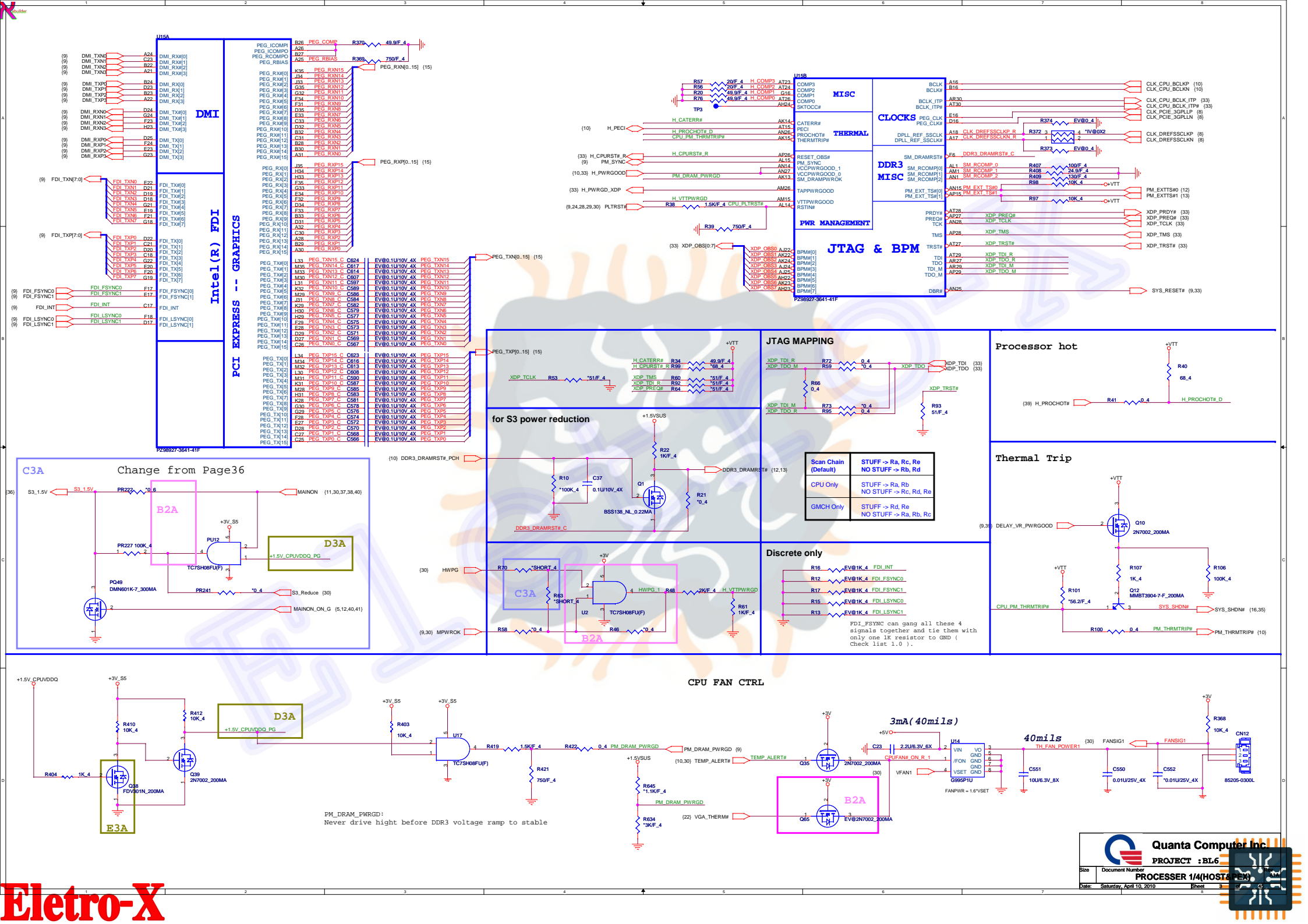
CLK POWERGOOD
Change to +3VPCU
(follow CRB)



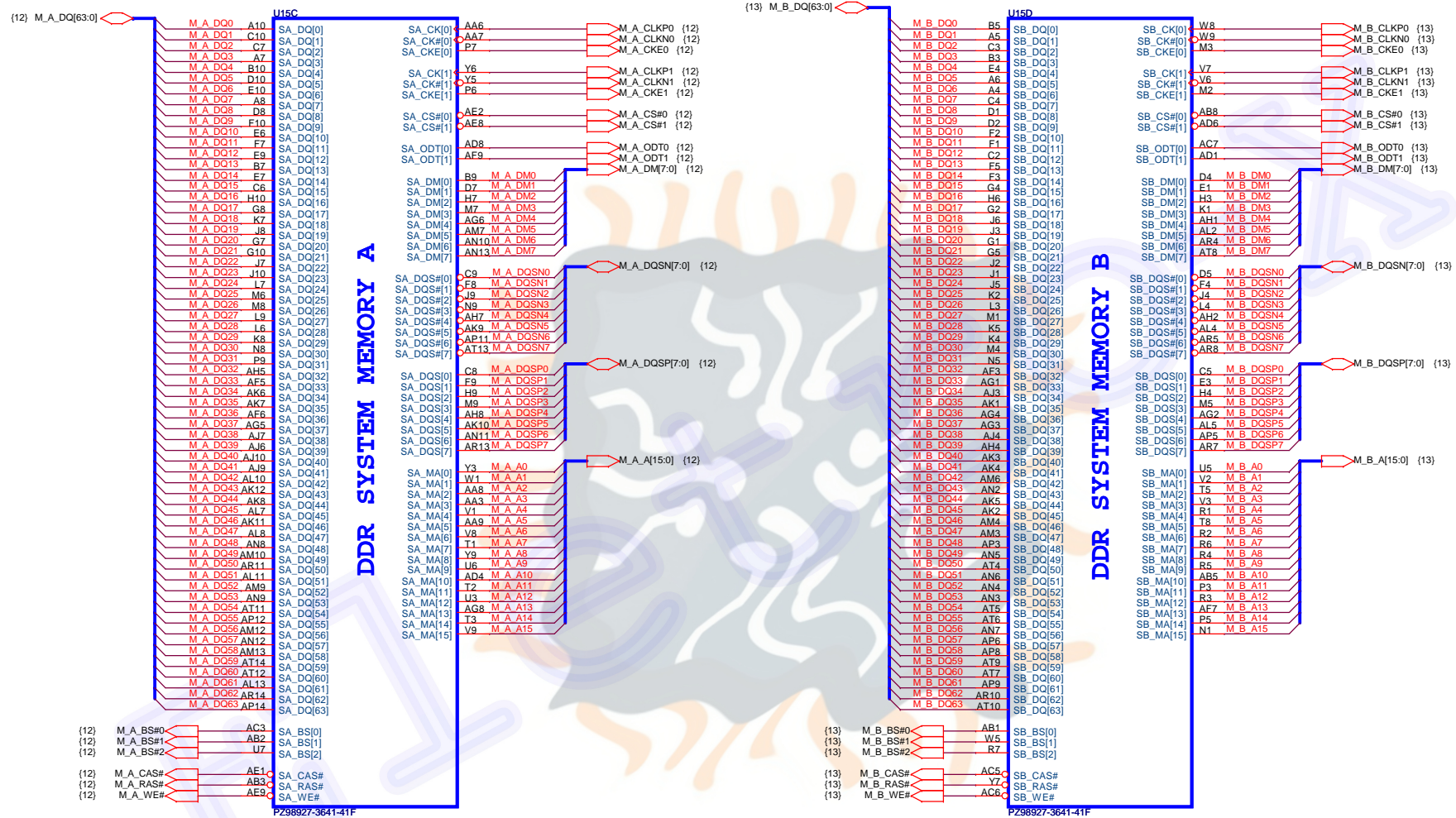
Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	CLOCK GENERATOR	A1A
Date:	Thursday, April 06, 2010	Sheet 2 of 45



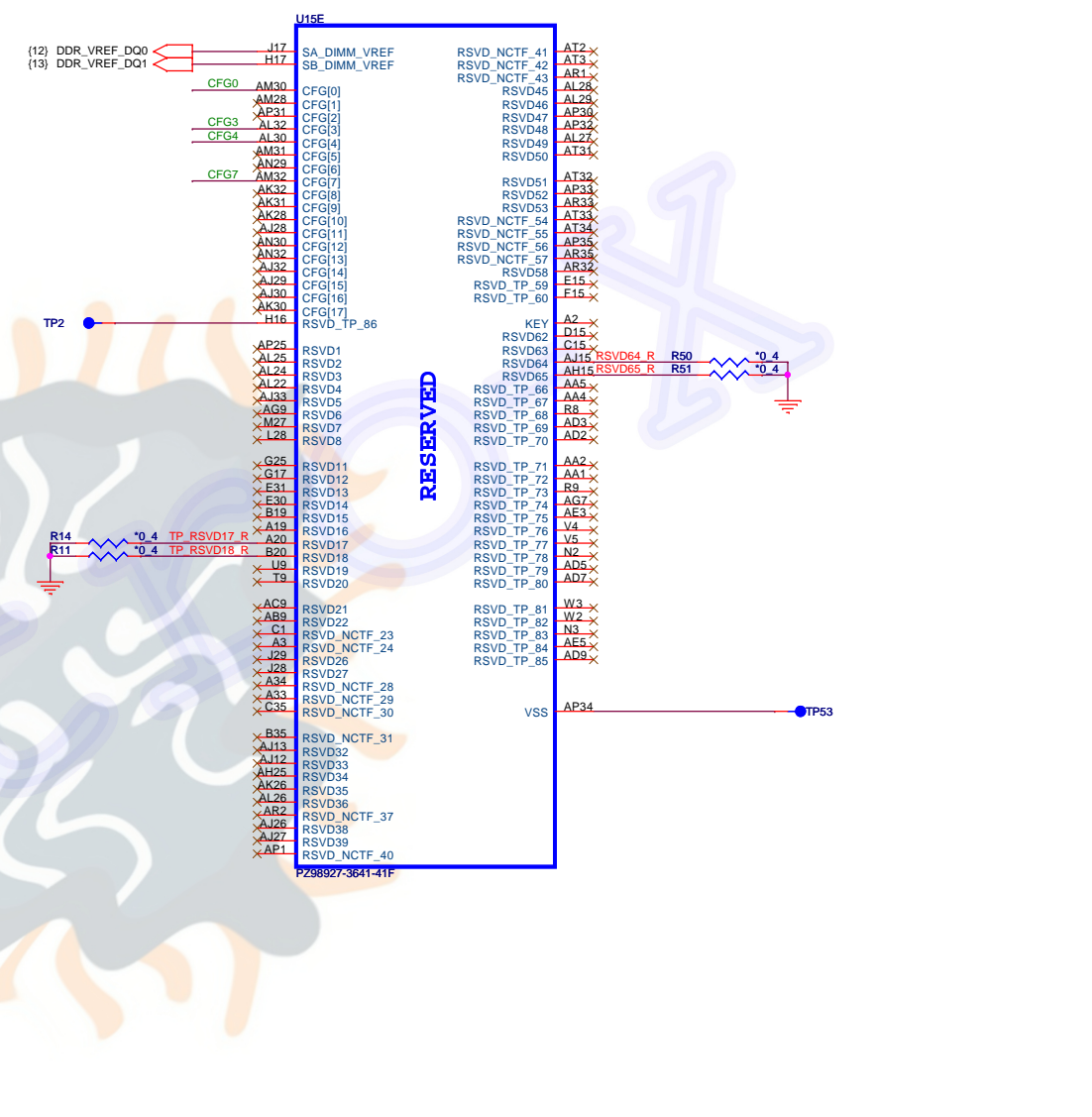
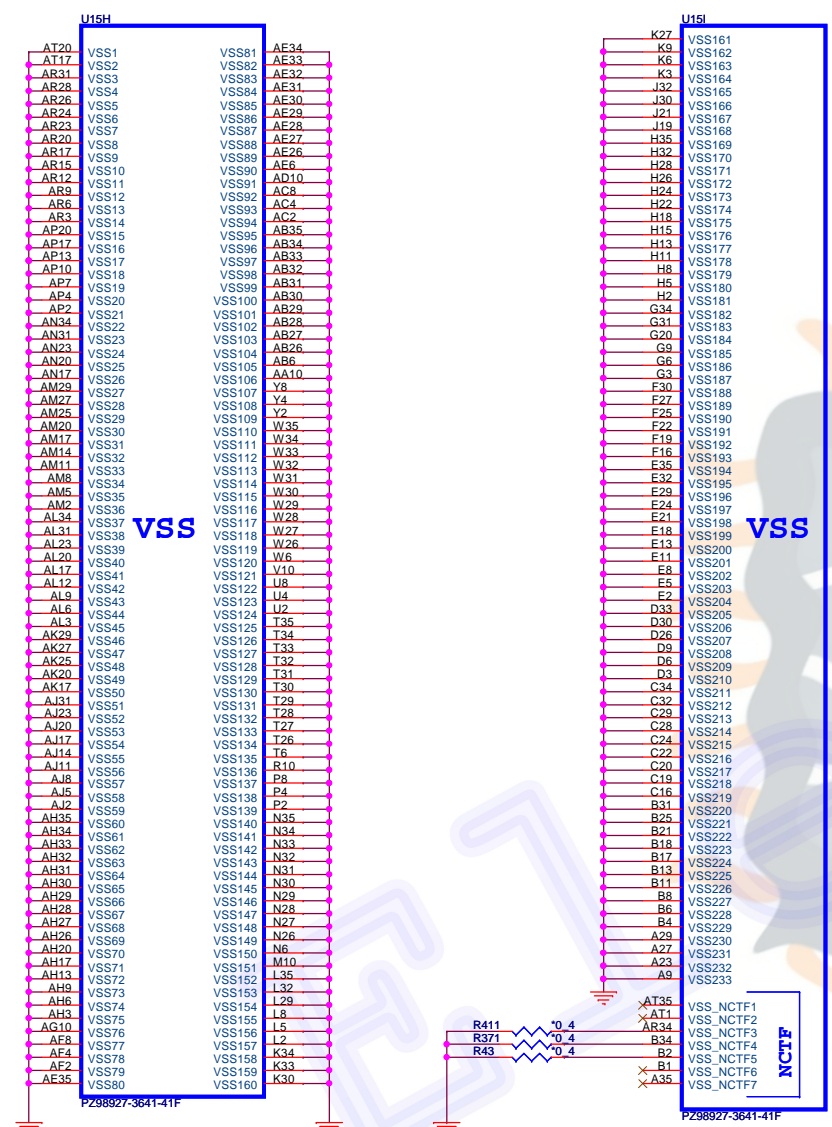


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

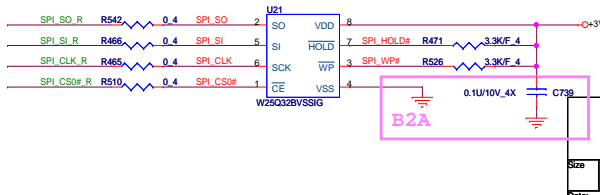
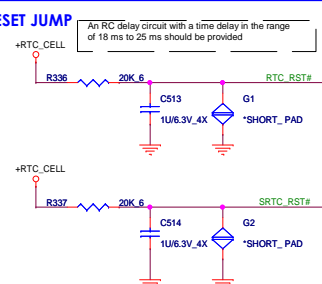
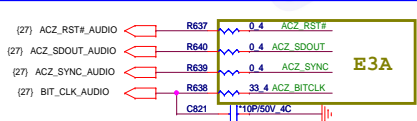
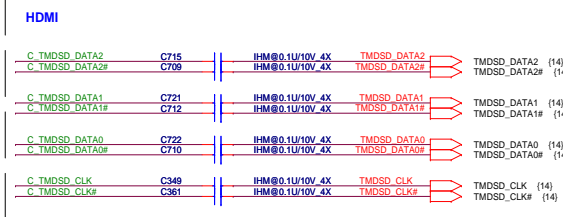
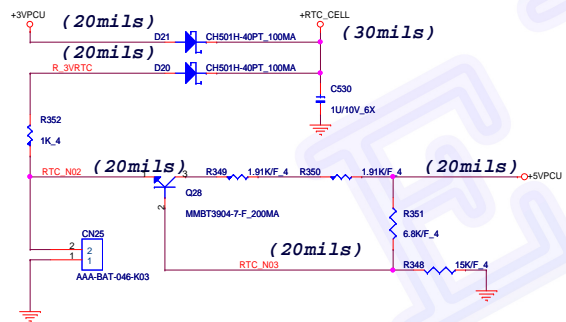
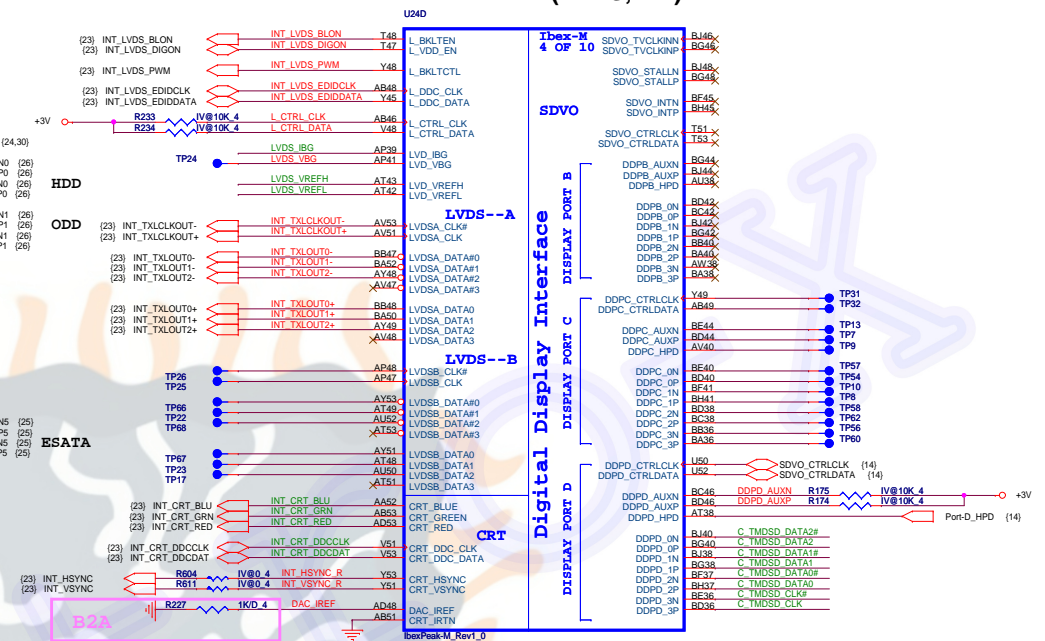
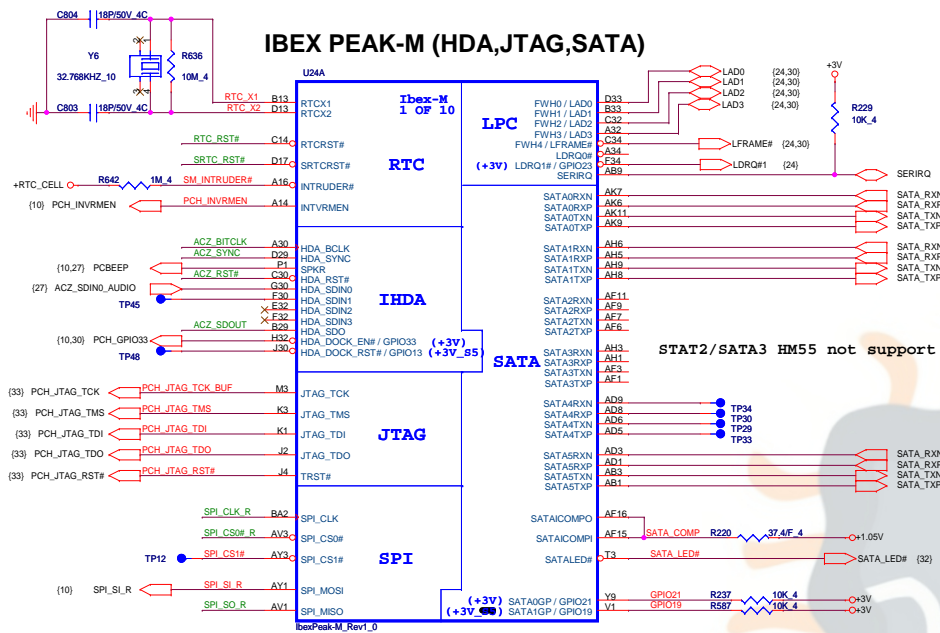



Quanta Computer Inc.

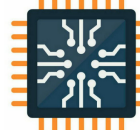
PROJECT : BL6

PROCESSOR 4/4 (GND)

Size: Document Number: Date: Saturday, April 10, 2010 Sheet: 6 of 6

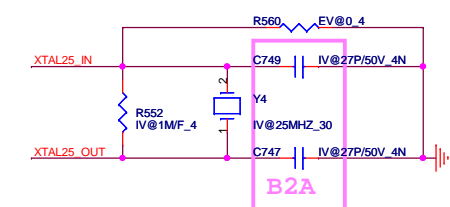
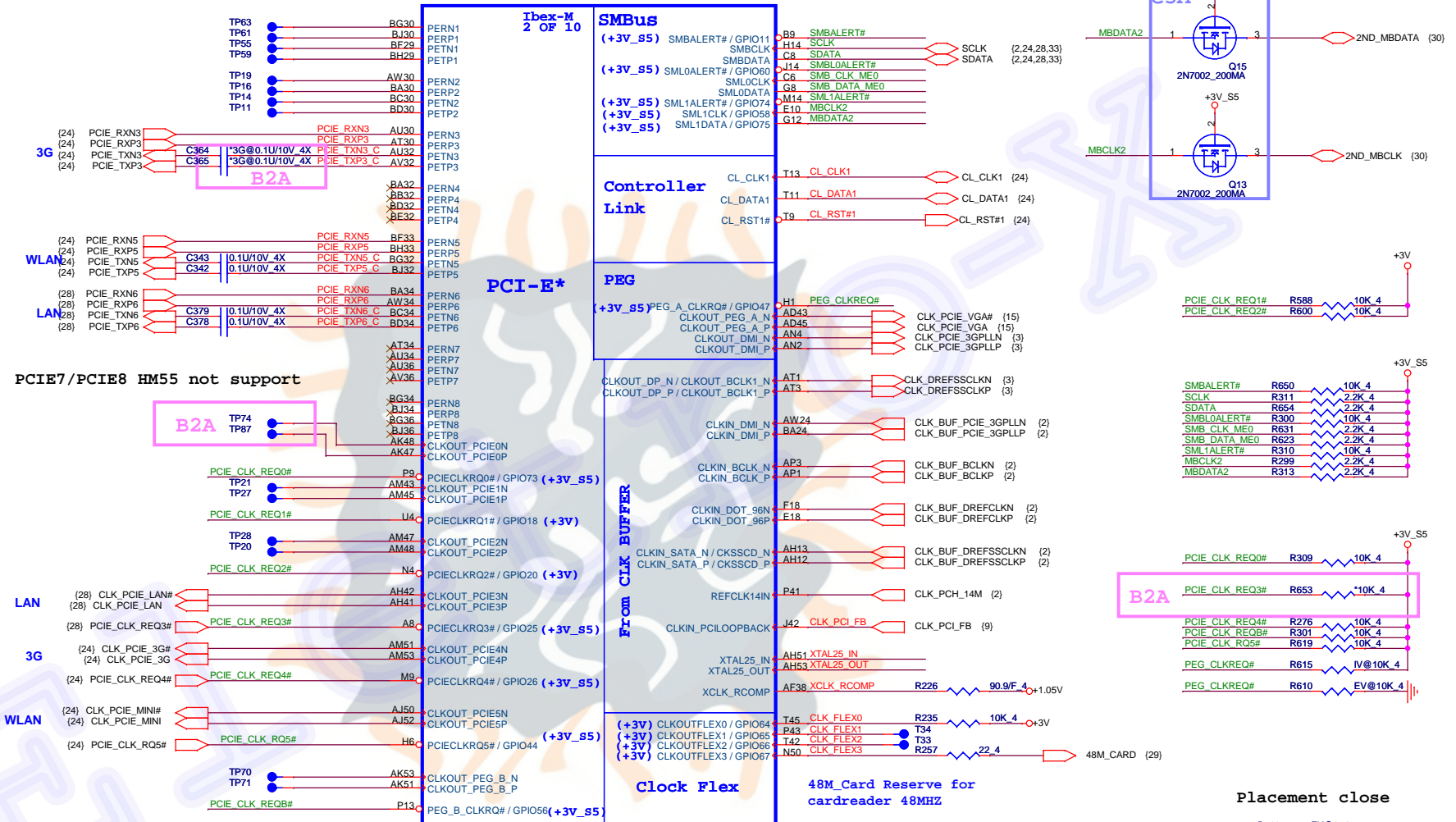



Quanta Computer Inc.
PROJECT : BL6
 Document Number **PCH 1/5 (SATA,HDA,LPC)** Rev A1
 Saturday, April 10, 2010 Sheet 7 of 45



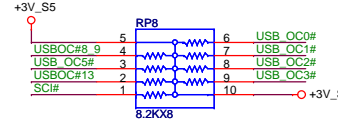
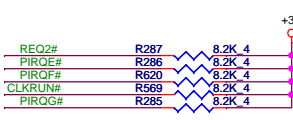
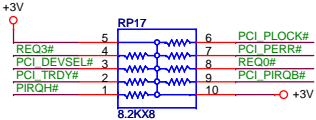
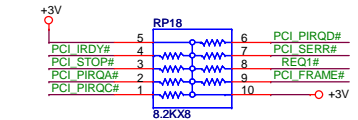
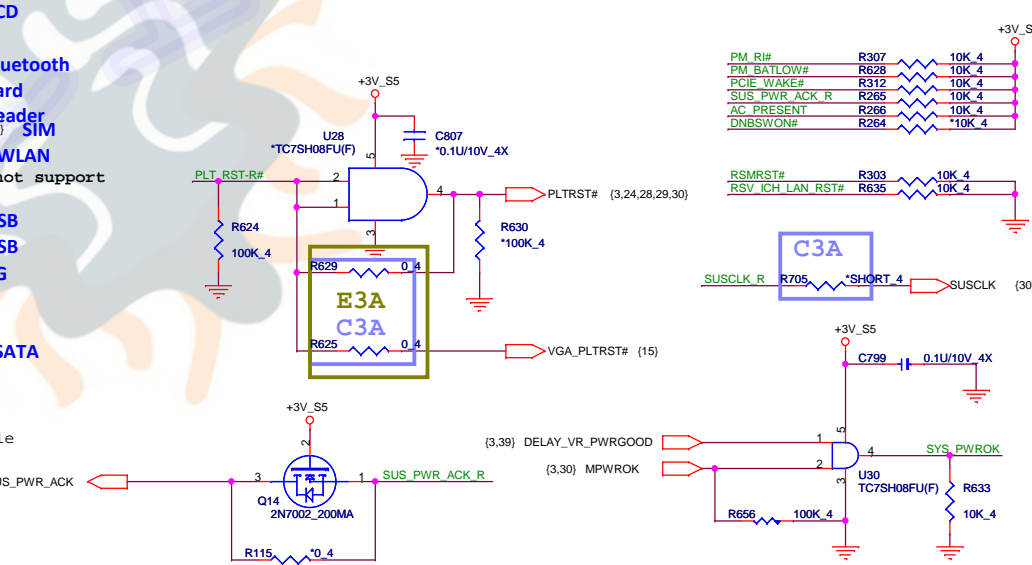
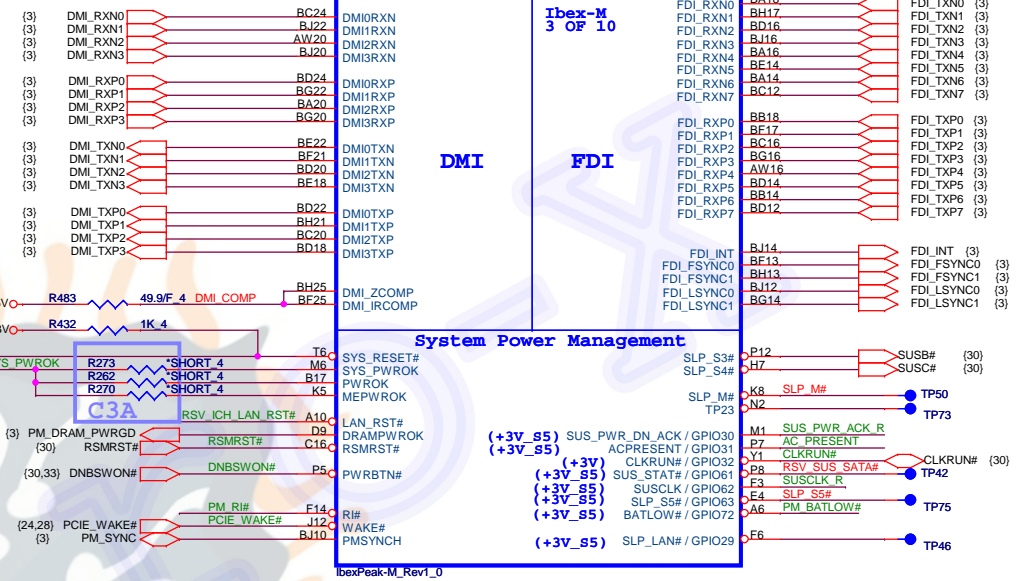
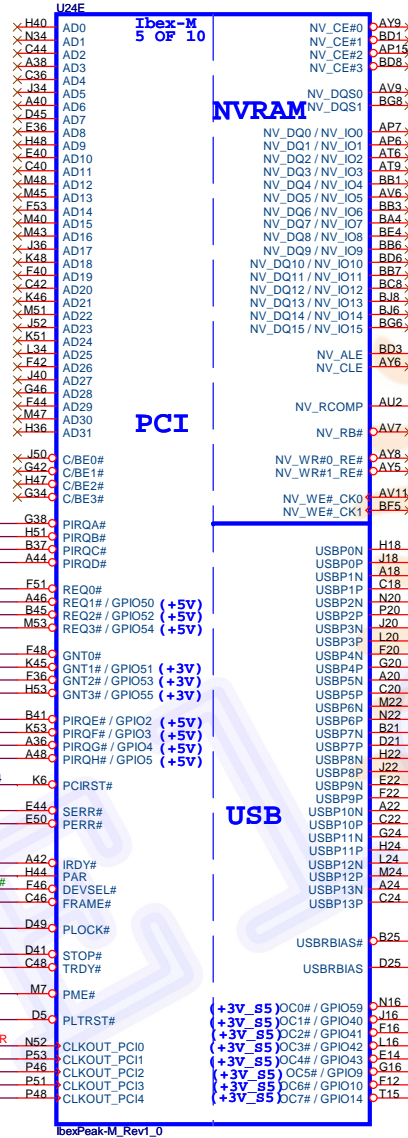
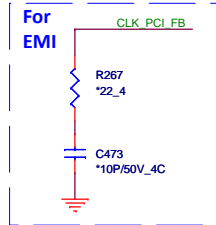
A7	VSS159	VSS259	H49
B11	VSS160	VSS260	H5
B15	VSS161	VSS261	J24
B19	VSS162	VSS262	K11
B23	VSS163	VSS263	K12
B31	VSS164	VSS264	K47
B35	VSS165	VSS265	K43
B39	VSS166	VSS266	L14
B43	VSS167	VSS267	L18
B47	VSS168	VSS268	L22
B612	VSS169	VSS269	L32
B812	VSS170	VSS270	L36
B816	VSS172	VSS272	L62
B820	VSS173	VSS273	M12
B830	VSS174	VSS274	M16
B834	VSS175	VSS275	M20
B838	VSS176	VSS276	N38
B842	VSS177	VSS277	M34
B846	VSS178	VSS278	M42
B85	VSS179	VSS279	M46
BC10	VSS180	VSS280	M22
BC14	VSS181	VSS281	M42
BC18	VSS182	VSS282	M49
BC2	VSS183	VSS283	M5
BC22	VSS184	VSS284	M24
BC32	VSS185	VSS285	P11
BC36	VSS186	VSS286	AD15
BC40	VSS187	VSS287	P22
BC44	VSS188	VSS288	P30
BC52	VSS189	VSS289	P30
BH3	VSS190	VSS290	P34
BD48	VSS191	VSS291	P42
BD49	VSS192	VSS292	P45
BD5	VSS193	VSS293	P25
BD5	VSS194	VSS294	P47
BE16	VSS195	VSS295	R52
BE20	VSS196	VSS296	T12
BE24	VSS197	VSS297	T41
BE30	VSS199	VSS299	T46
BE34	VSS200	VSS300	T49
BE38	VSS201	VSS301	T5
BE42	VSS202	VSS302	T8
BE46	VSS203	VSS303	U30
BE48	VSS204	VSS304	U31
BE50	VSS205	VSS305	U32
BE5	VSS206	VSS306	U33
BE8	VSS207	VSS307	V18
BF3	VSS208	VSS308	P16
BF49	VSS209	VSS309	V19
BF51	VSS210	VSS310	V20
BG18	VSS211	VSS311	V30
BG24	VSS212	VSS312	V30
BG4	VSS213	VSS313	V32
BG50	VSS214	VSS314	V32
BH11	VSS215	VSS315	V31
BH15	VSS216	VSS316	V34
BH19	VSS217	VSS317	V35
BH23	VSS218	VSS318	V37
BH31	VSS219	VSS319	V43
BH35	VSS220	VSS320	V45
BH39	VSS221	VSS321	V46
BH43	VSS222	VSS322	V47
BH47	VSS223	VSS323	V48
BH7	VSS224	VSS324	V7
C12	VSS225	VSS325	V15
C50	VSS226	VSS326	V8
D61	VSS227	VSS327	W2
E12	VSS228	VSS328	W52
E16	VSS229	VSS329	Y11
E20	VSS230	VSS330	Y12
E24	VSS231	VSS331	Y15
E30	VSS232	VSS332	Y20
E34	VSS233	VSS333	Y23
E38	VSS234	VSS334	Y30
E42	VSS235	VSS335	Y31
E46	VSS236	VSS336	Y32
E48	VSS237	VSS337	Y31
E6	VSS238	VSS338	Y38
E49	VSS239	VSS339	V46
F5	VSS240	VSS340	P49
G10	VSS241	VSS341	Y5
G14	VSS242	VSS342	Y24
G18	VSS243	VSS343	Y6
G2	VSS244	VSS344	Y8
G22	VSS245	VSS345	T43
G32	VSS246	VSS346	AD51
G36	VSS247	VSS347	AT8
G39	VSS248	VSS348	AD47
G40	VSS249	VSS349	AD7
G50	VSS250	VSS350	AD12
AF39	VSS251	VSS351	AM6
H16	VSS252	VSS352	AT13
H20	VSS253	VSS353	AT15
H30	VSS254	VSS354	AM35
H34	VSS255	VSS355	AK45
H38	VSS256	VSS356	AV19
H42	VSS257	VSS356	
H46	VSS258		

U24B



IBEX PEAK-M (+DMI,FDI,GPIO)

IBEX PEAK-M (PCI,USB,NVRAM)



Quanta Computer Inc

PROJECT : BL6

PCH 3/5 (PCI,ONFI,USB,DMI)

Date: Saturday, April 10, 2010

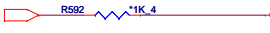
Sheet 9 of 9

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)


PCH Strap Pin Configuration Table

SPKR

(7,27) PCBEEP  R592 *1K_4 +3V


Reboot option at power-up
0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/
GPIO55

(9) GNT3#  R622 *10K_4 +3V

Top-Block
Swap Override
0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

HDA_DOCK_EN
#GPIO33

(7,30) PCH_GPIO33  R282 *1K_4 +3V

Flash Descriptor
Security Override
0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

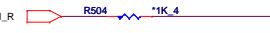
GNT0#,
GNT1#

(9) GNT0#  R272 *1K_4 +3V

(9) GNT1#  R621 *1K_4 +3V

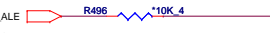
Boot BIOS Strap		
PCI_GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

SPI_MOSI

(7) SPI_SI_R  R504 *1K_4 +3V

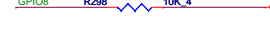
TPM Functionality
Disable
1 = Enabled
0 = Disable

NV_ALE

(9) NV_ALE  R496 *10K_4 +1.8V

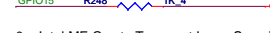
IntelR Anti-Theft Technology
HDD Data Protection
(Intel AT-d) Enable
1 = Enabled
0 = Disabled (Default)

GPIO8

 R298 *10K_4 +3V_S5

Reserved
This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

 R248 *1K_4 +3V_S5

Reserved
0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

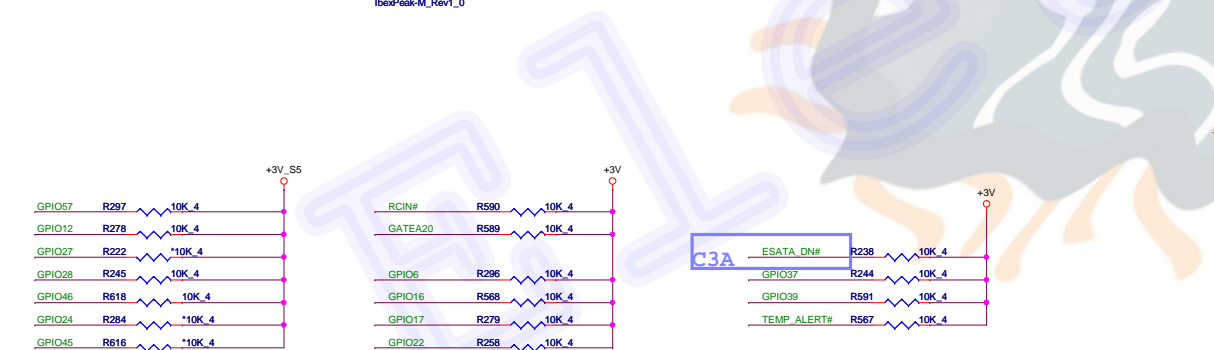
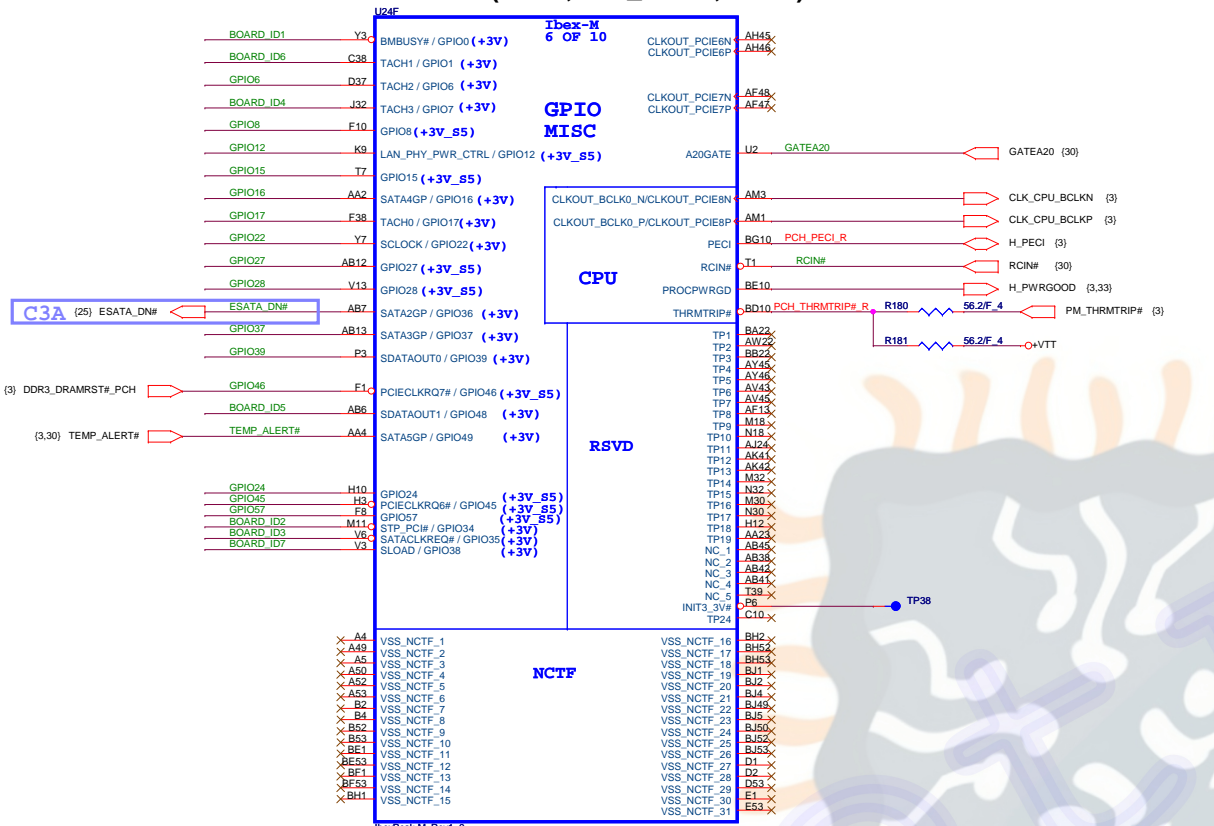
GPIO27

 R232 *10K_4 +3V

On-Die PLL Voltage
Regulator
0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails.
No need to use on-board filter circuit.
This signal has a weak internal pull-up.

+RTC_CELL  R644 *330K_6 PCH_INVRMEN

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

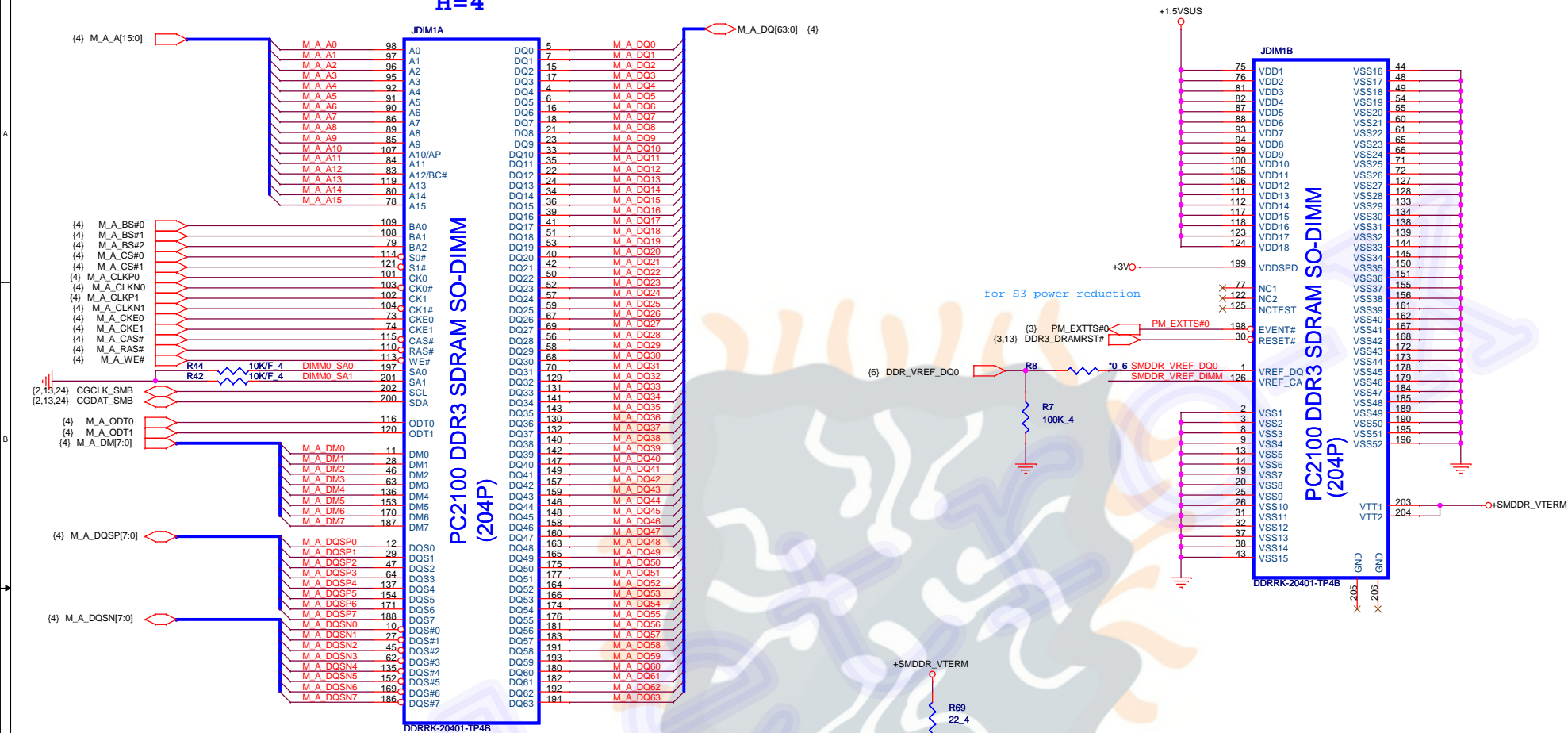


BOARD ID SETTING

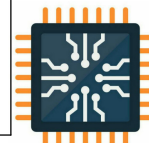
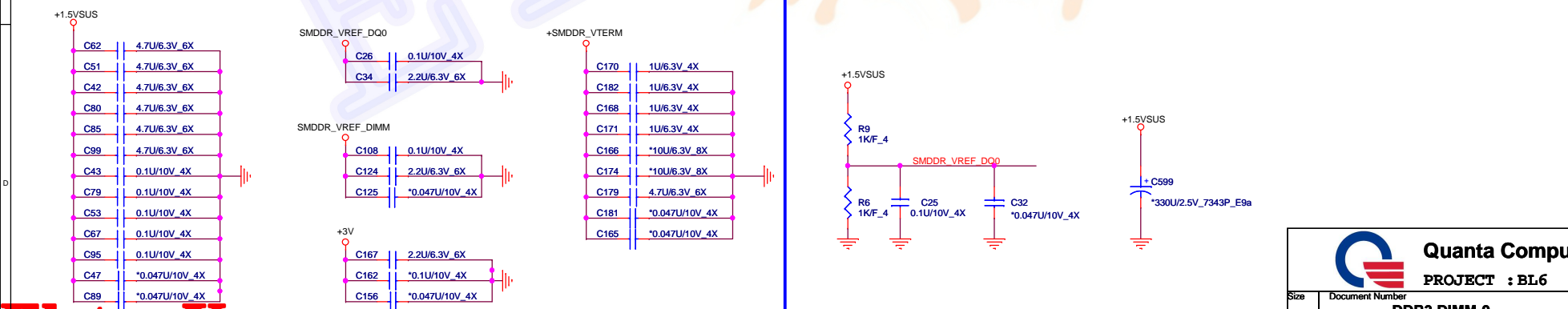
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU VGA SKU	H	L					
W/ MDC W/O MDC			H	L			
W/ HDMI W/O HDMI			H	L			
W/O 3G W/ 3G				H	L		
15" 14"					H	L	
W/O BT W/ BT					H	L	

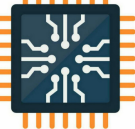
Electro-X

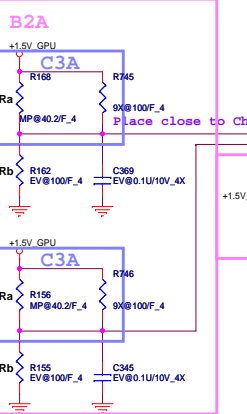
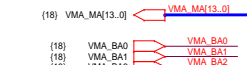
H=4



Place these Caps near So-Dimm0.



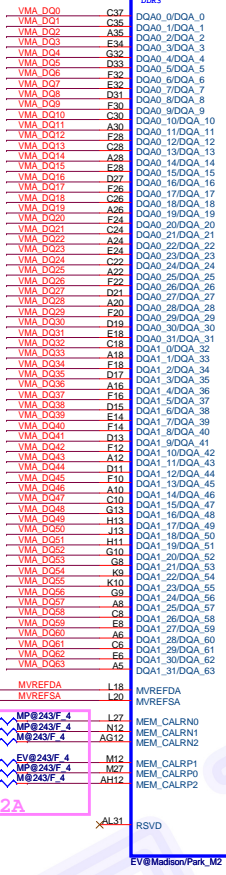




DDR3/GDDR3 Memory Stuff Option			
Madison/Park	GDDR3	DDR3	
MVDDQ	1.8V/1.5	1.5V	
Ra	40.2R	40.2R	
Rb	100R	100R	

M96/M92	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	100R
Rb	100R	100R

C3A



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

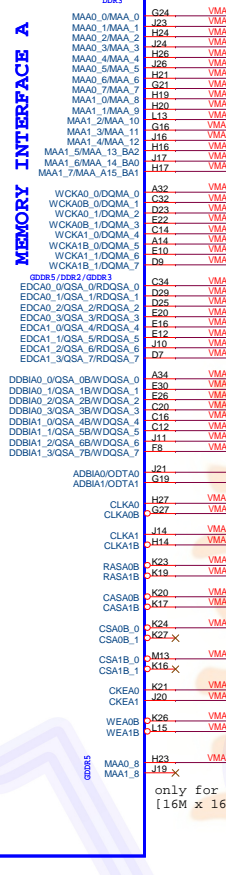
EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

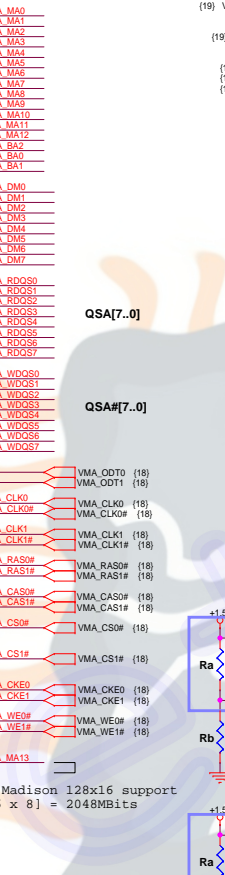
EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

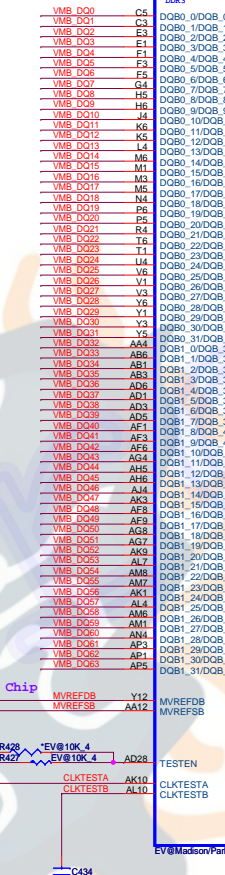
EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

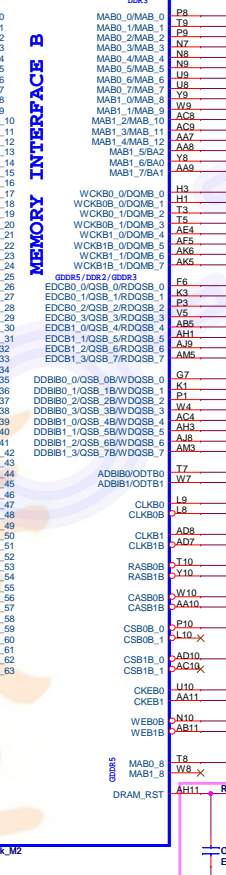
EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

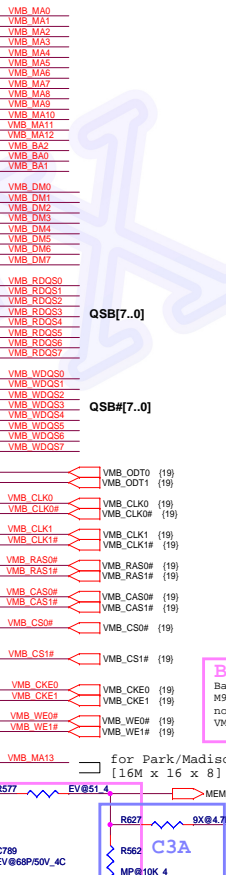
EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

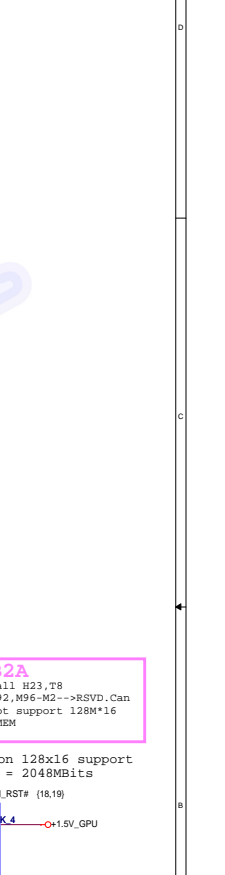
EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2



EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

EV@MadisonPark_M2

Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V	V		
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V	V		

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

CHANNEL A: 512MB DDR3 (64M*16*4pcs)

TOP Left

Group-A0 VREF

MEM_A0 CLK

Group-A0 decoupling CAP

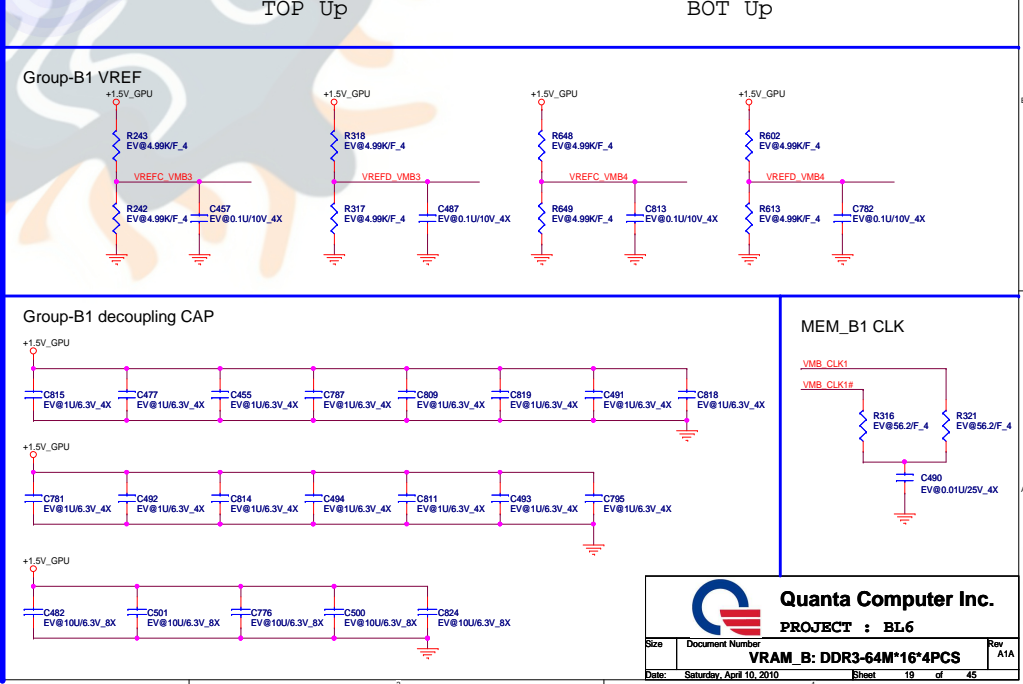
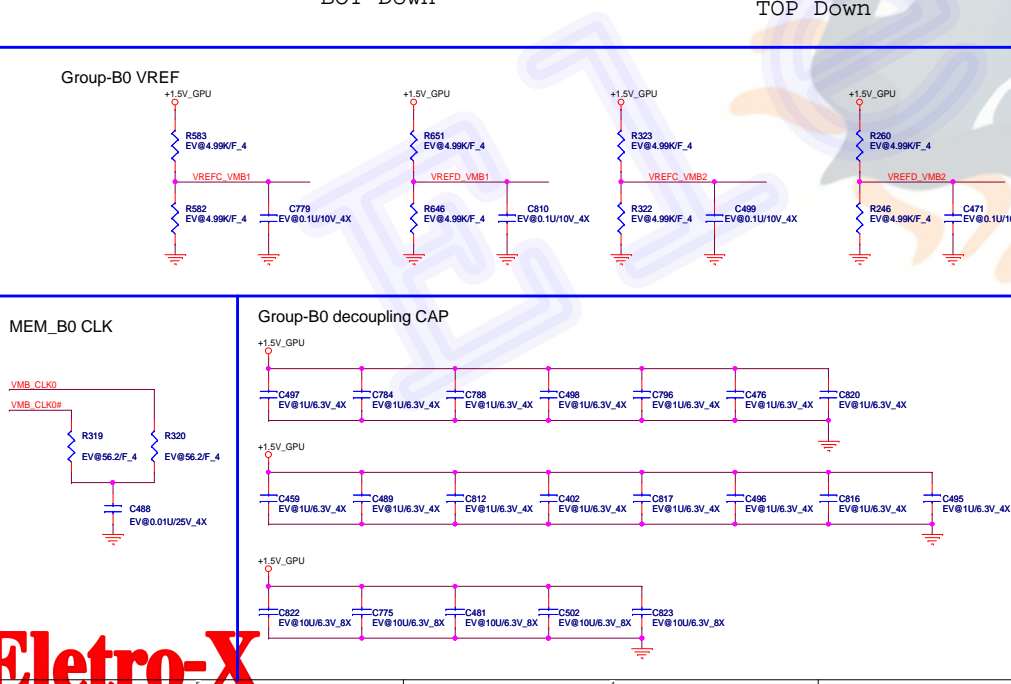
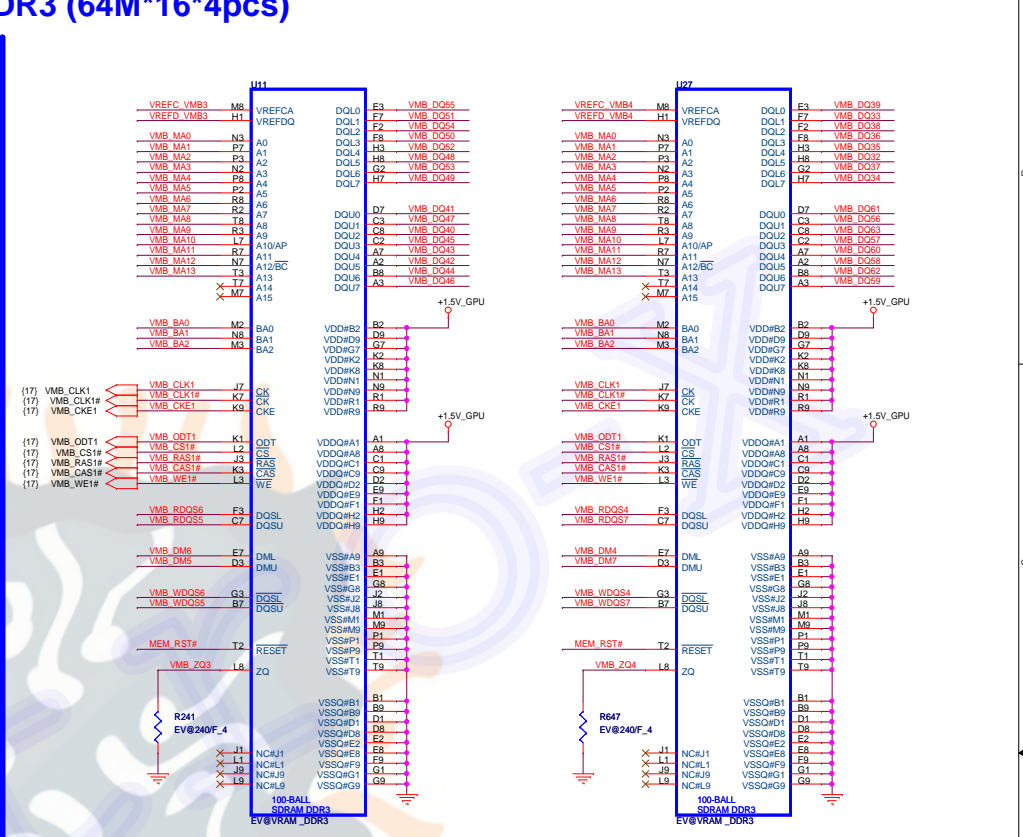
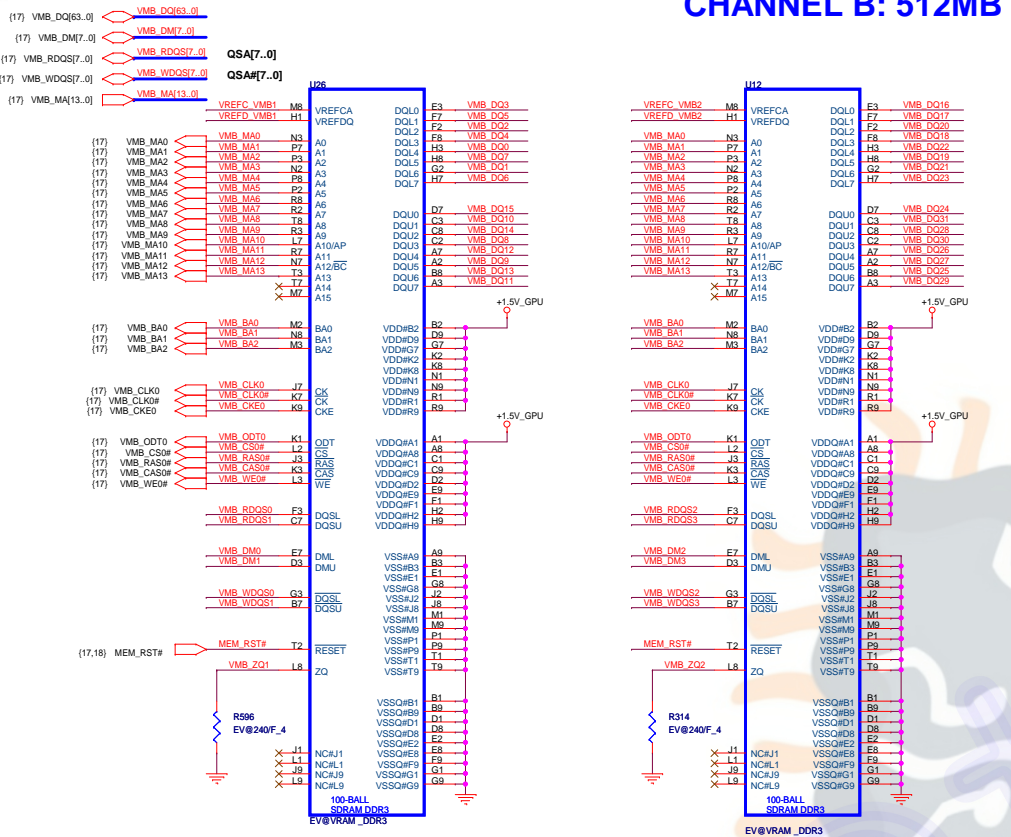
Group-A1 VREF

Group-A1 decoupling CAP

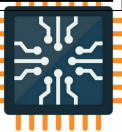
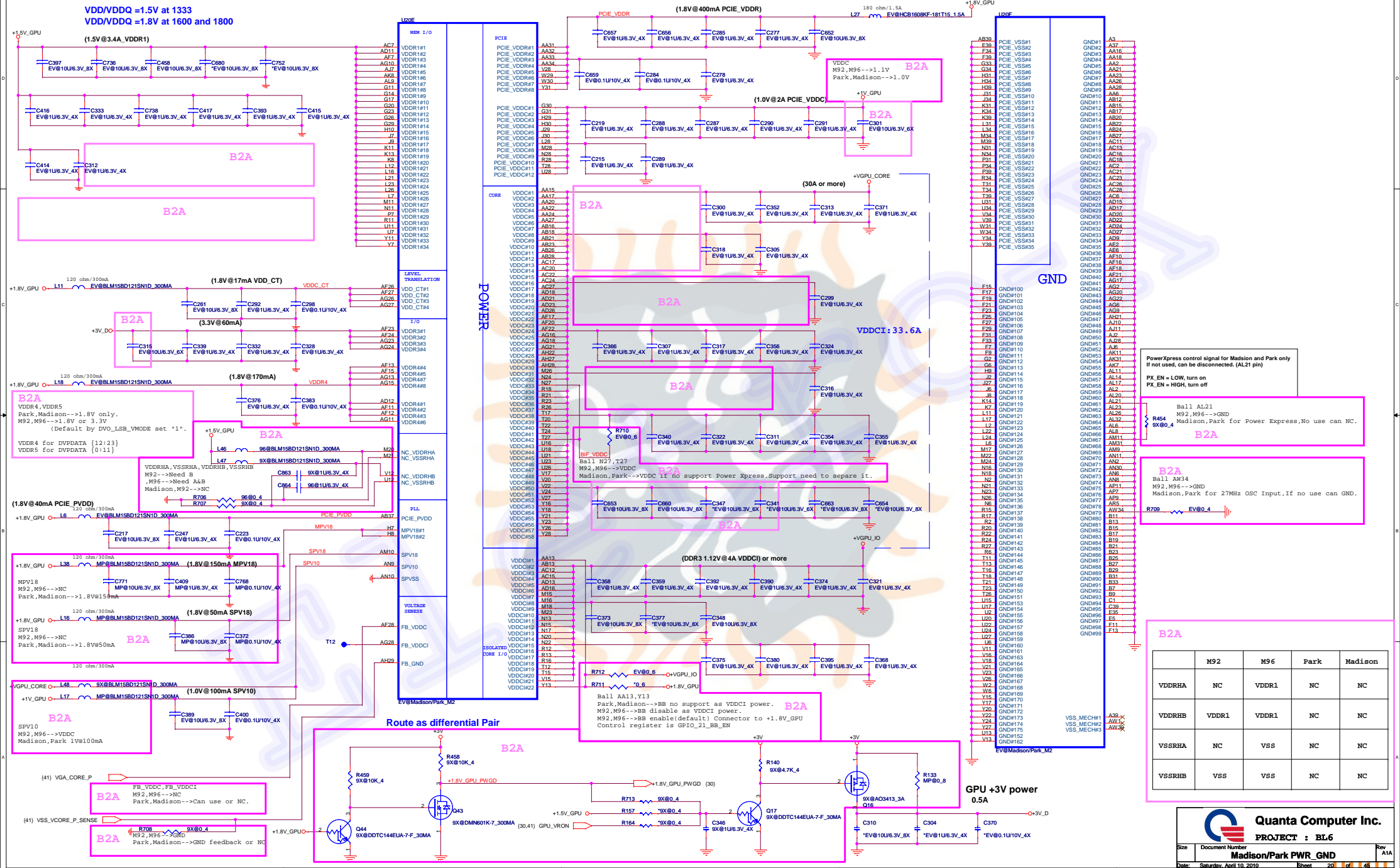
MEM_A1 CLK

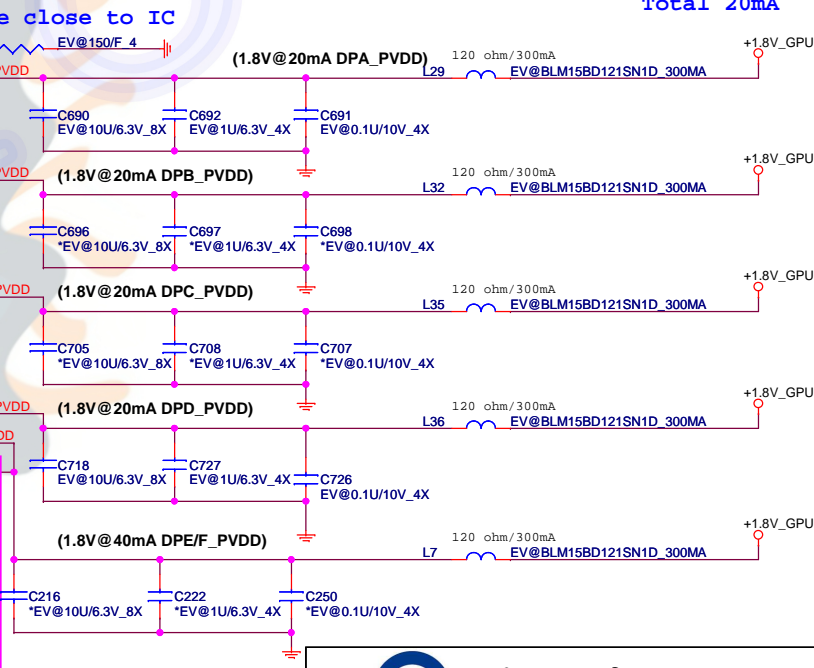
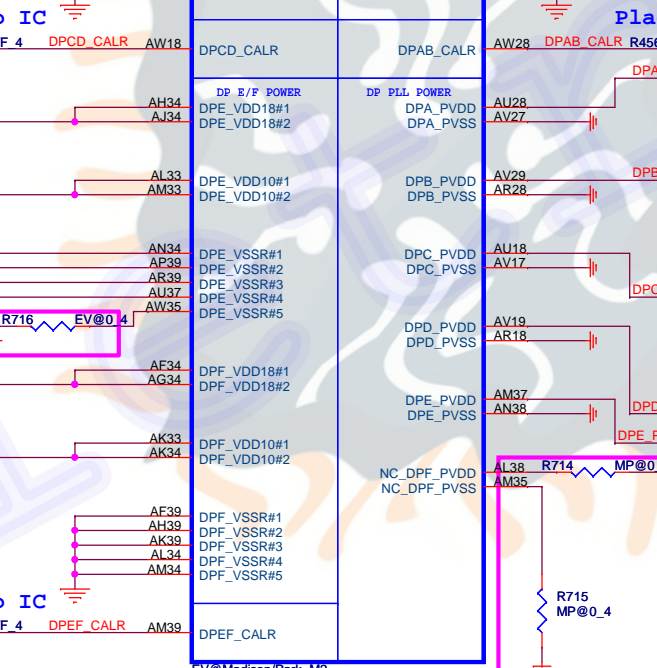
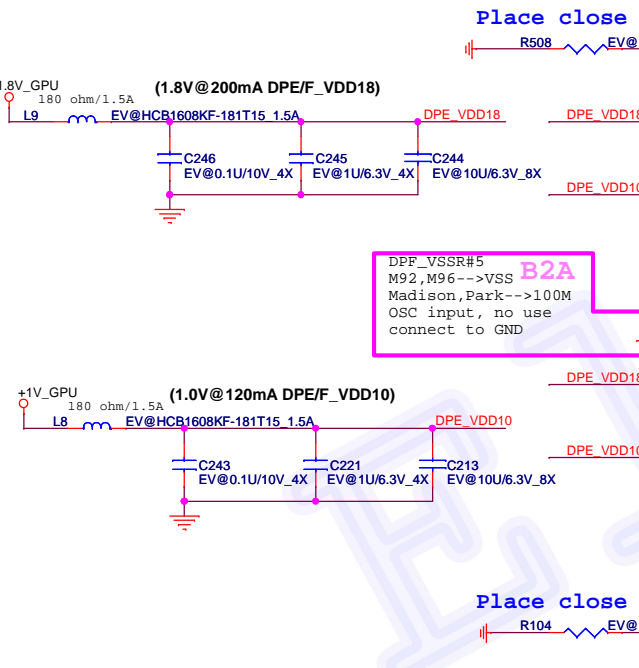
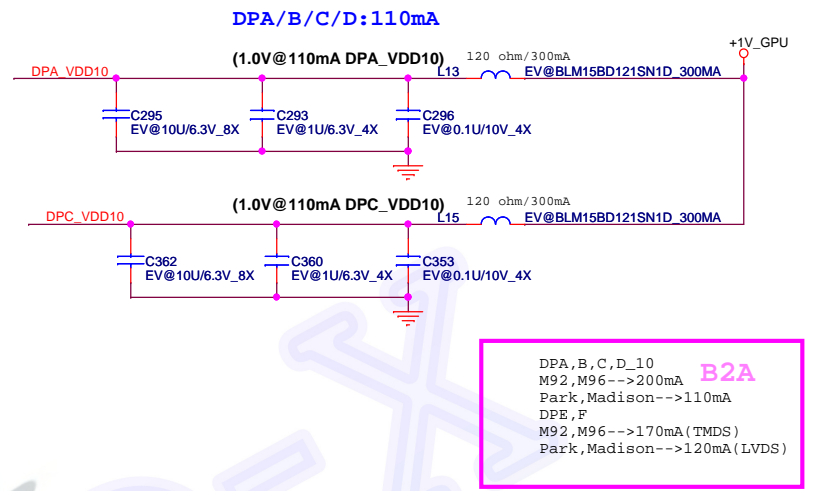
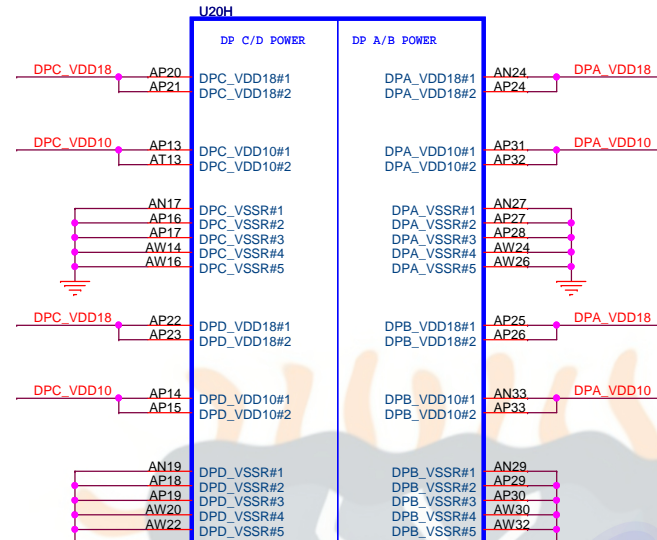
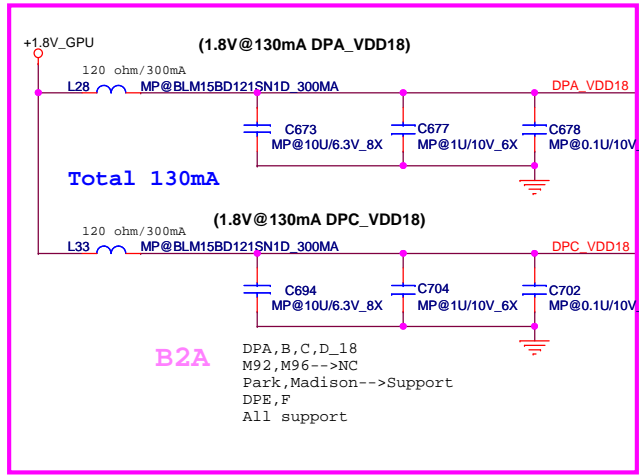
Quanta Computer Inc.
PROJECT : BL6
Size: [] Document Number: []
Date: Saturday, April 10, 2010 Sheet 18 of 45

CHANNEL B: 512MB DDR3 (64M*16*4pcs)



For Madison and Park VDDCI and VDDC can share one common regulator





Quanta Computer Inc.

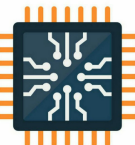
PROJECT : BL6

Size Document Number

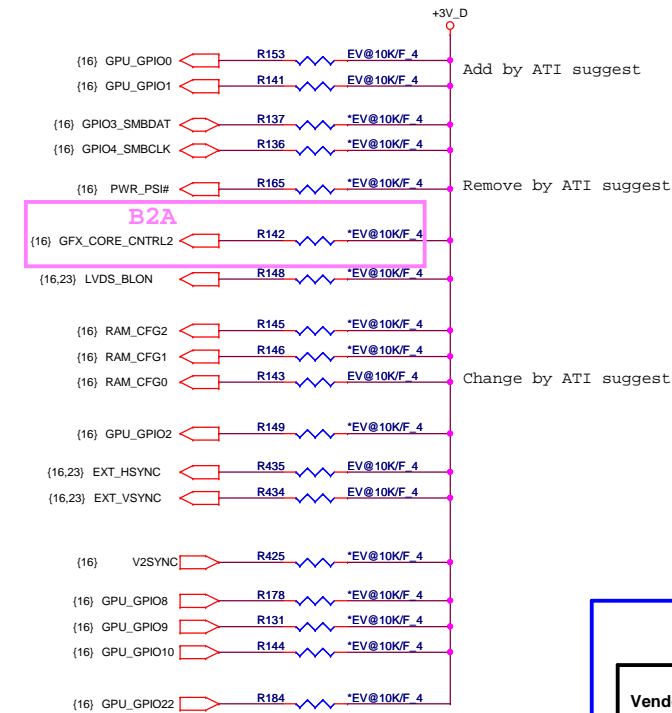
Madison/Park DPPW_GND

Date: Saturday, April 10, 2010 Sheet 21 of 45

Rev A1A



PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0] Size	
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

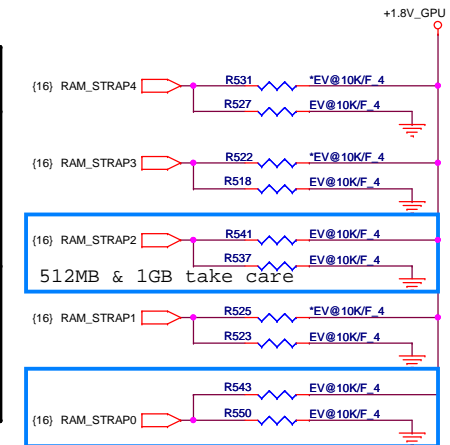
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

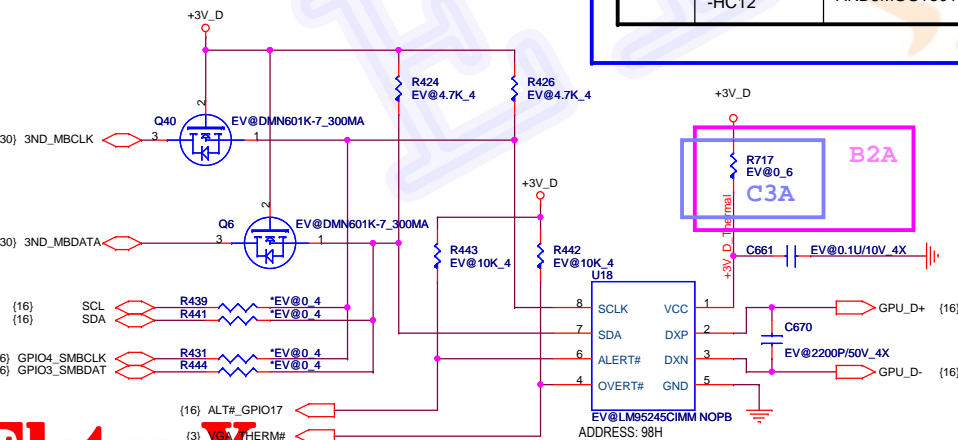
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

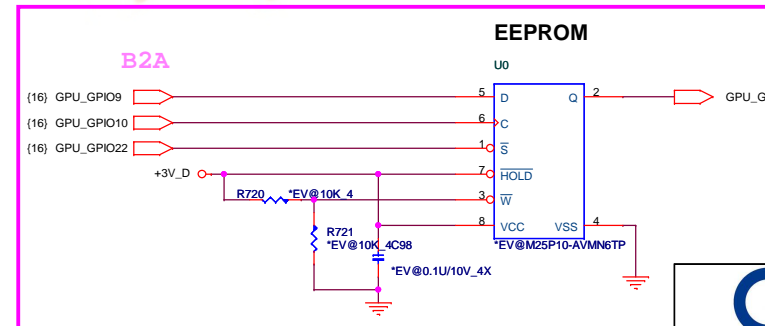
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
			2GB	0	0	1	1	0	1



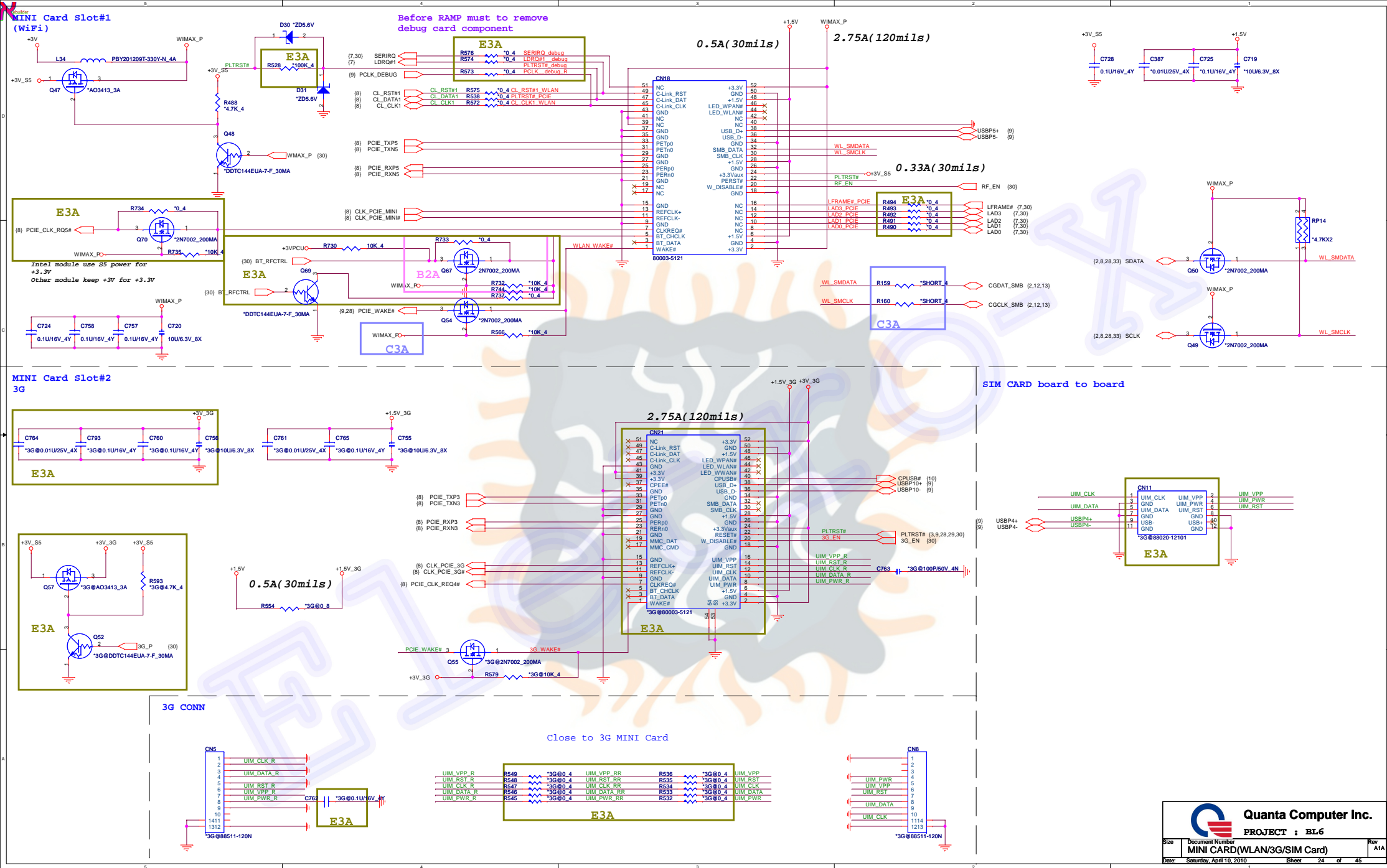
Thermal Sensor



EEPROM

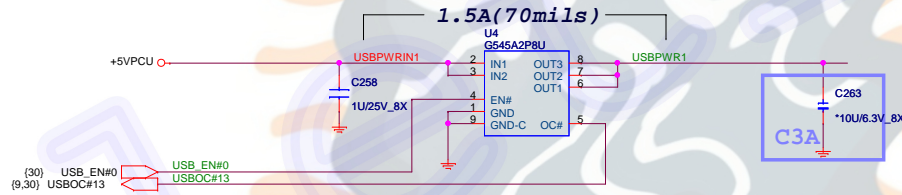
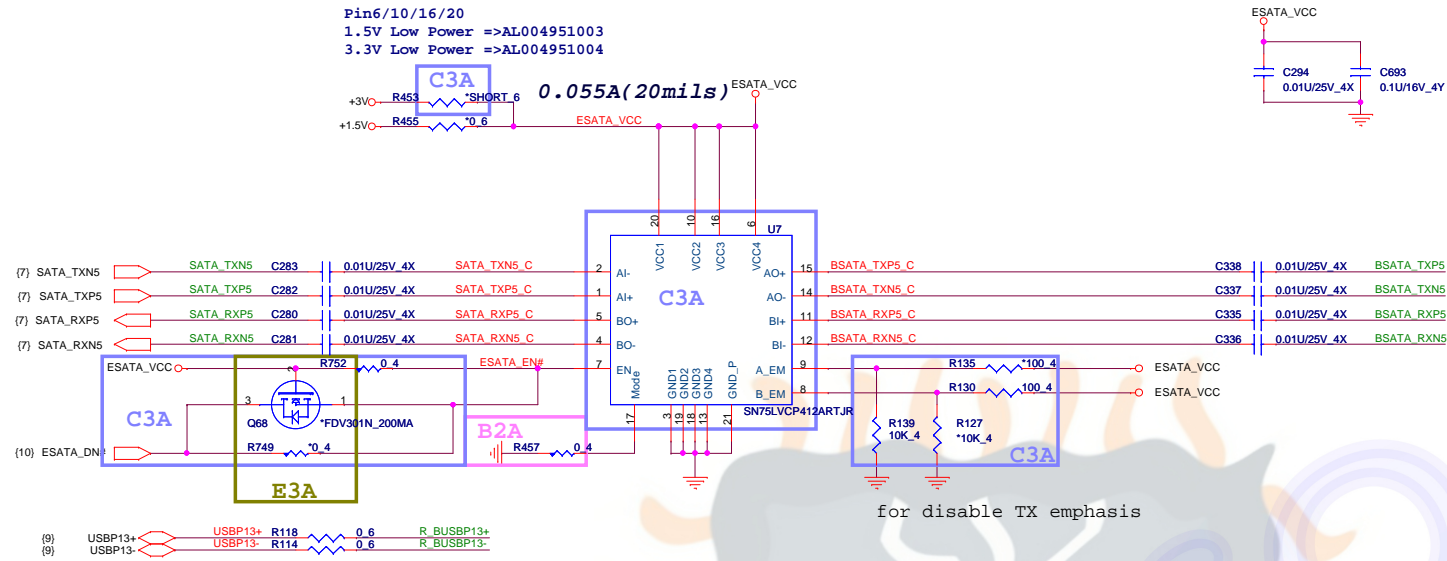


PROJECT : BL6
Memory strip/Thermal/HDMI

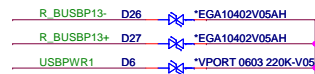
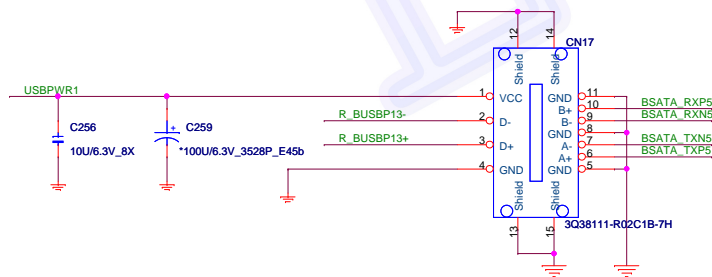


ESATA Re-driver IC

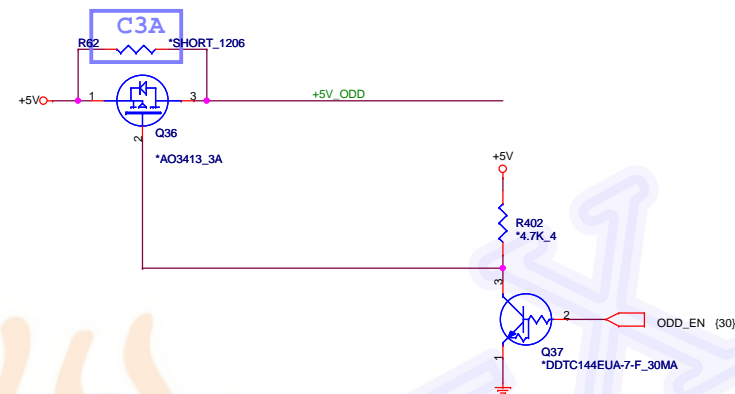
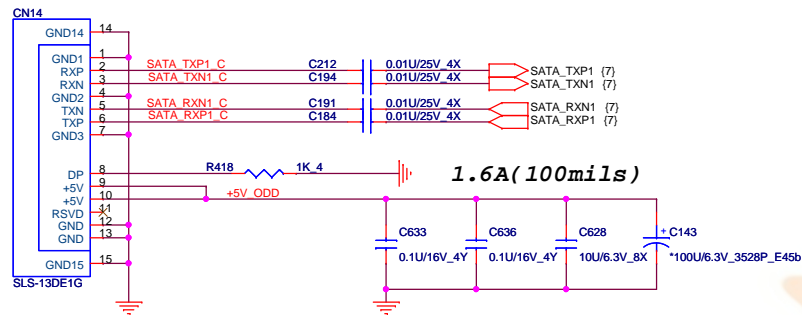
Pin6/10/16/20
1.5V Low Power =>AL004951003
3.3V Low Power =>AL004951004



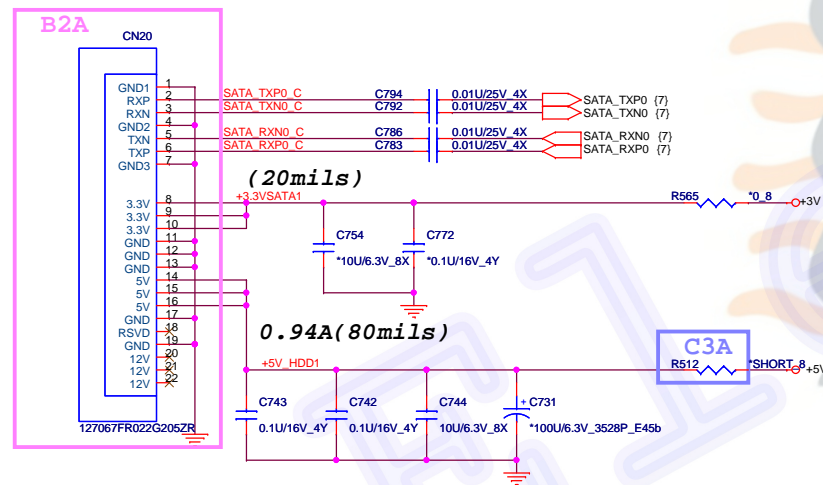
ESATA CONN



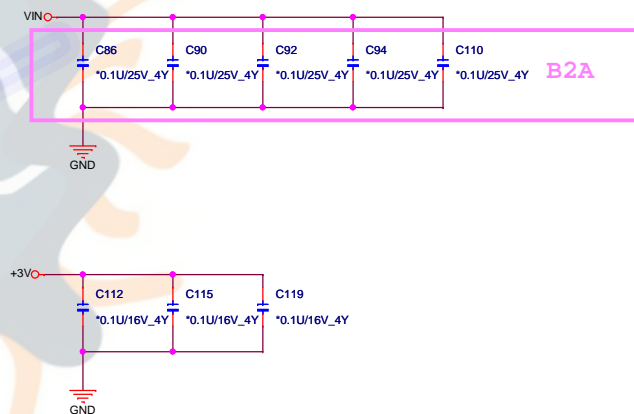
SATA ODD

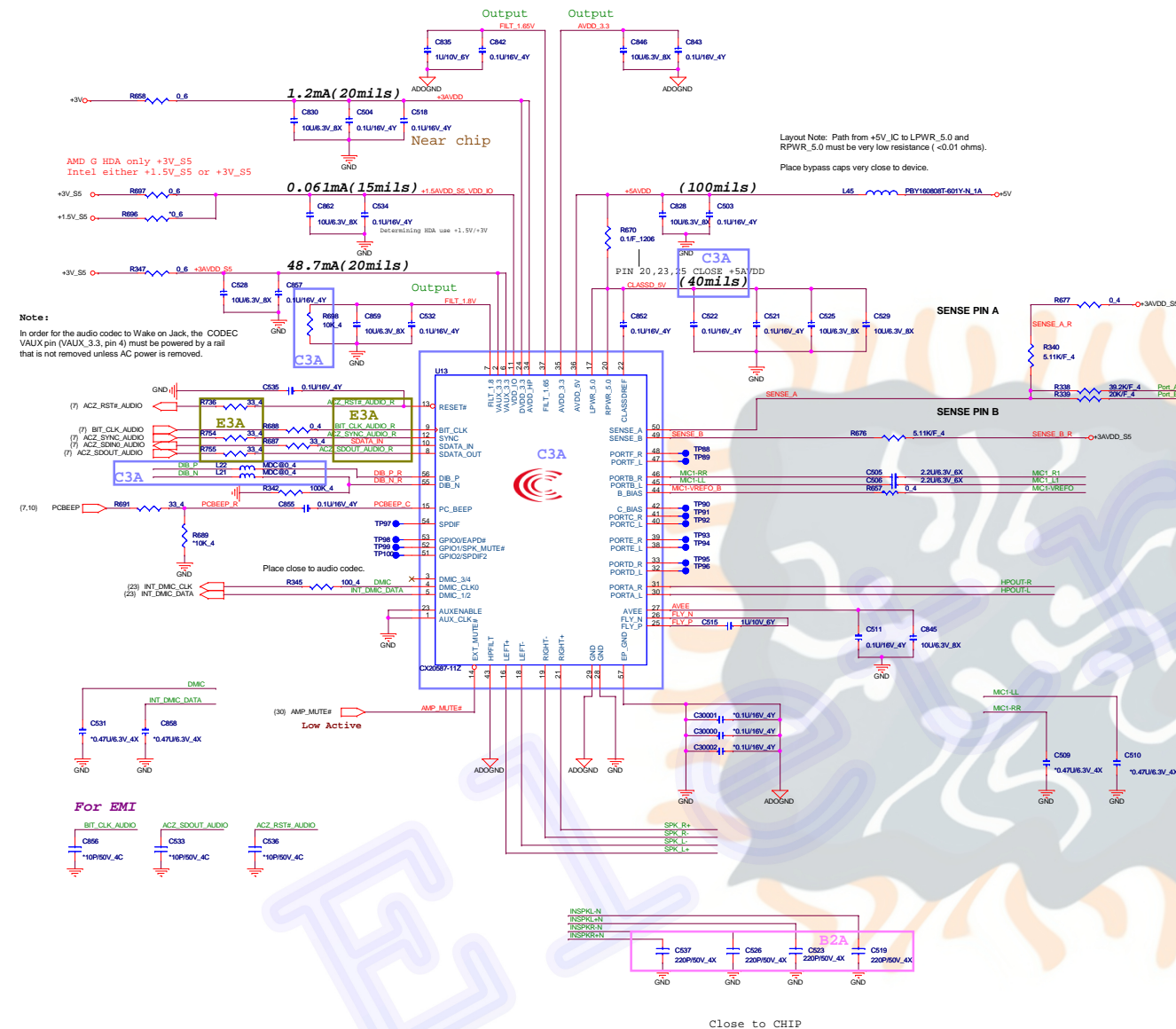


SATA HDD



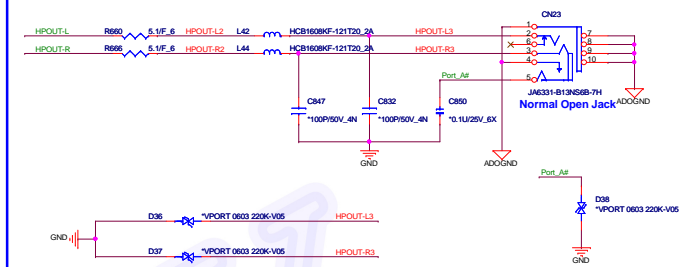
EMI



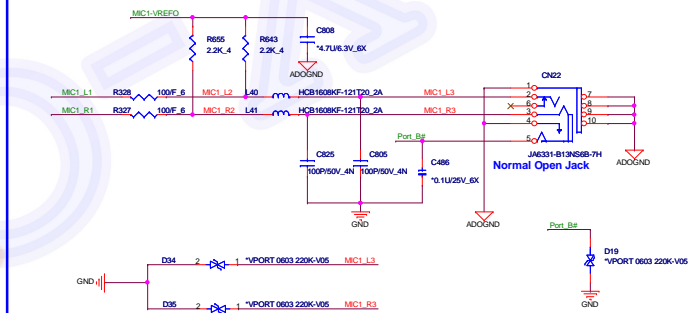


AUDIO JACKS

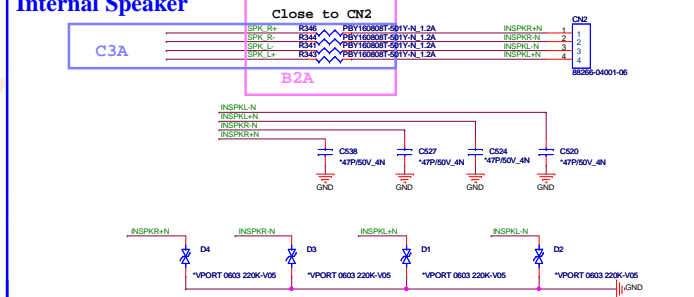
Earphone



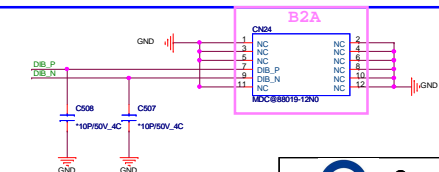
External MIC



Internal Speaker

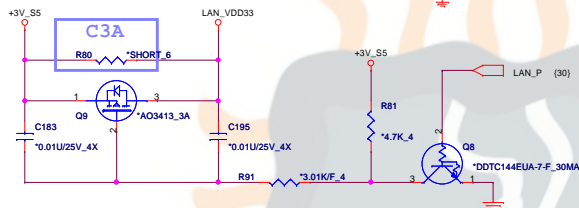
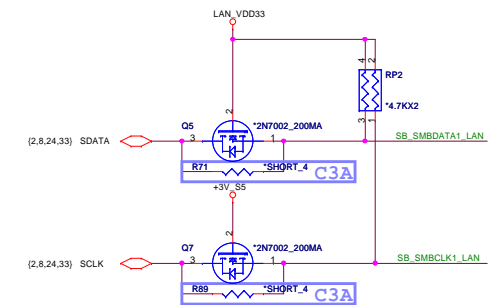
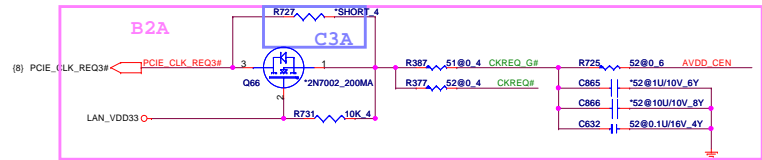


MDC

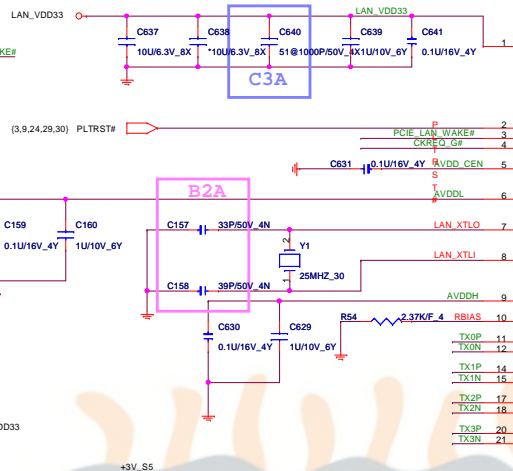


Atheros Lan

AMD mount Q66, NO mount R727
INTEL mount R727, NO mount Q66



0.163A(20mils)



Atheros

AR8151/AR8152

G
1
0G

/A
1:
0A
0R
:8
A1
R5
81
1-
5A
2L
-1
AA
L-
1R

A
-
=

R
J
4
5

A
R
A
=

A
0
A0
L8

A
R
A
=

A
0
A0
L8

A
R
A
=

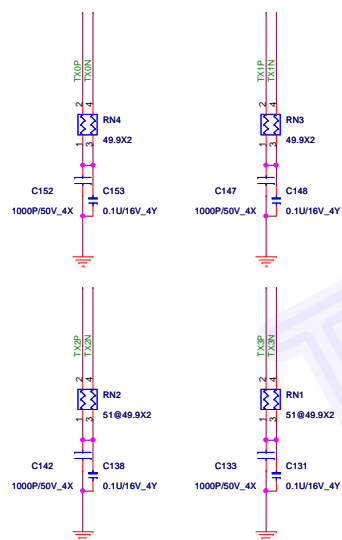
A
0
A0
L8

A
R
A
=

A
0
A0
L8

A
R
A
=

PLACE NEAR LAN IC SIDE



T
R
A
N
S
F
O
R
M
E
R

B2A

N551

C81

C655

C96

C669

C102

C759

C109

C3A

C3A

C3A

C3A

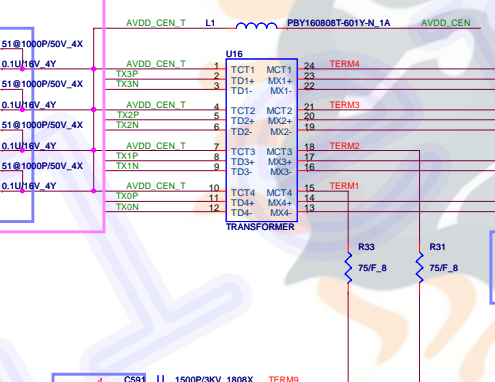
C3A

C3A

C3A

C3A

C3A



R27, R28
GIGA = 75 ohm
10/100 = 0 ohm

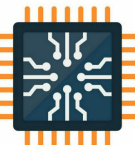
Quanta Computer Inc.
PROJECT : BL6

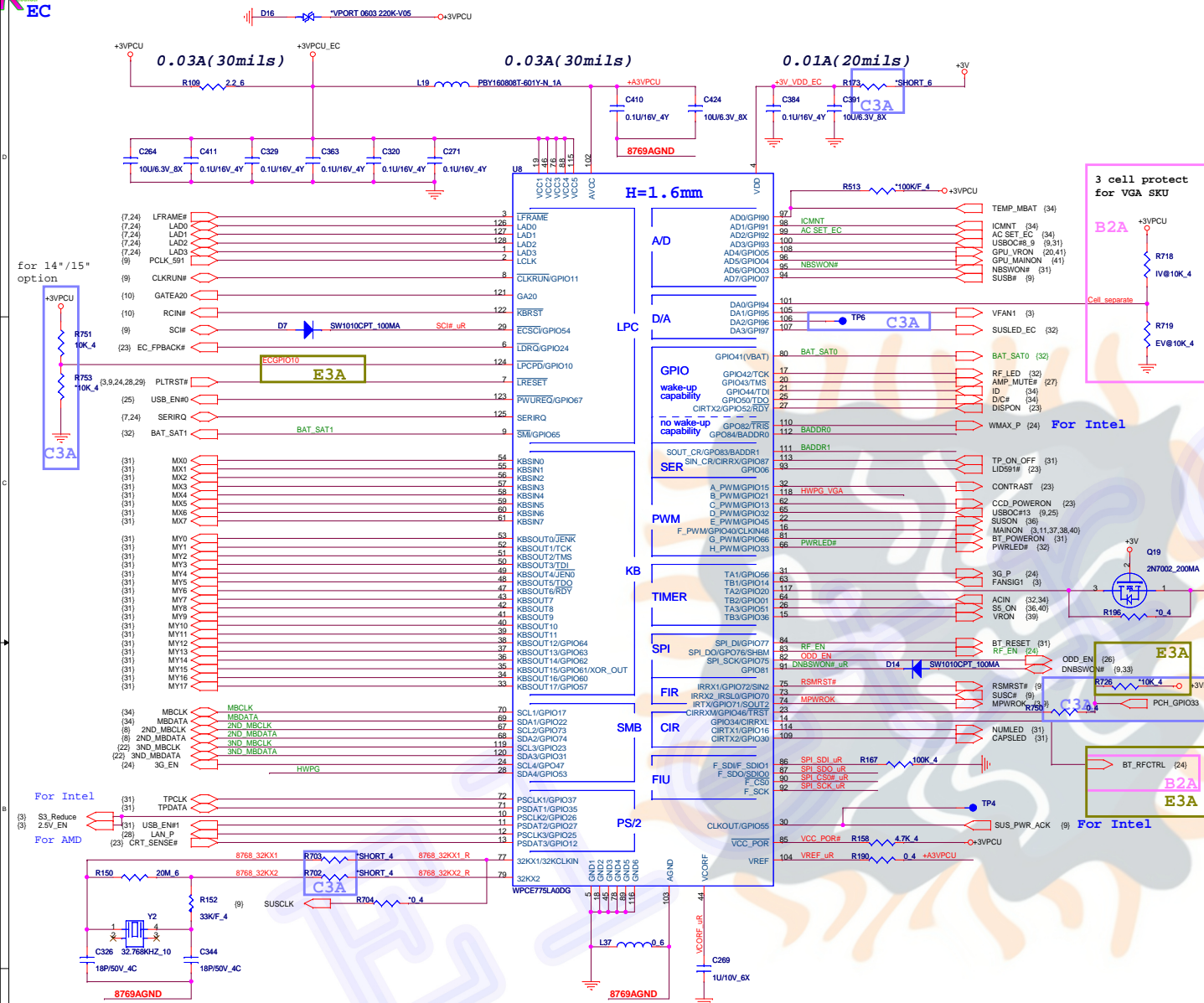
Size Document Number
Atheros Lan

Date: Saturday, April 10, 2010

Sheet 28 of 45

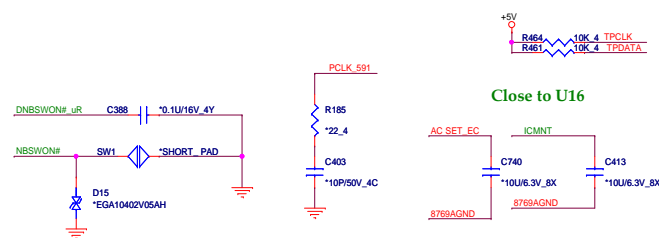
Rev A1A



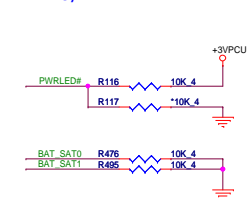


SMBUS Table

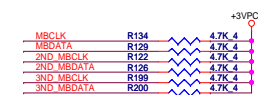
SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBUS	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H



LED PU/PD



SM BUS PU



I/O Base Address

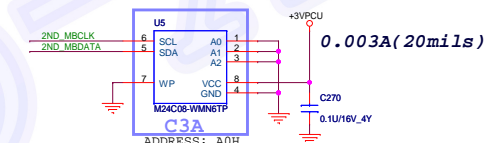
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MOD	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS



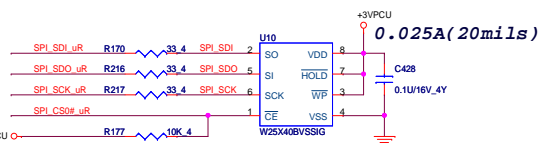
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware.

ID



SPI FLASH

For Intel

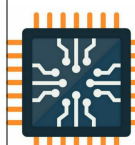
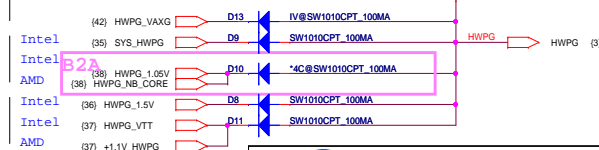
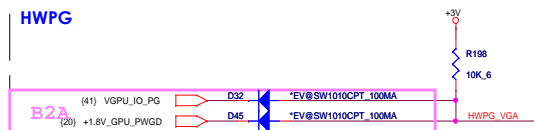


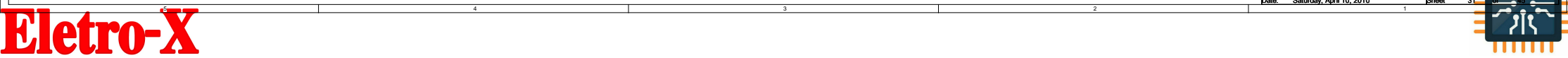
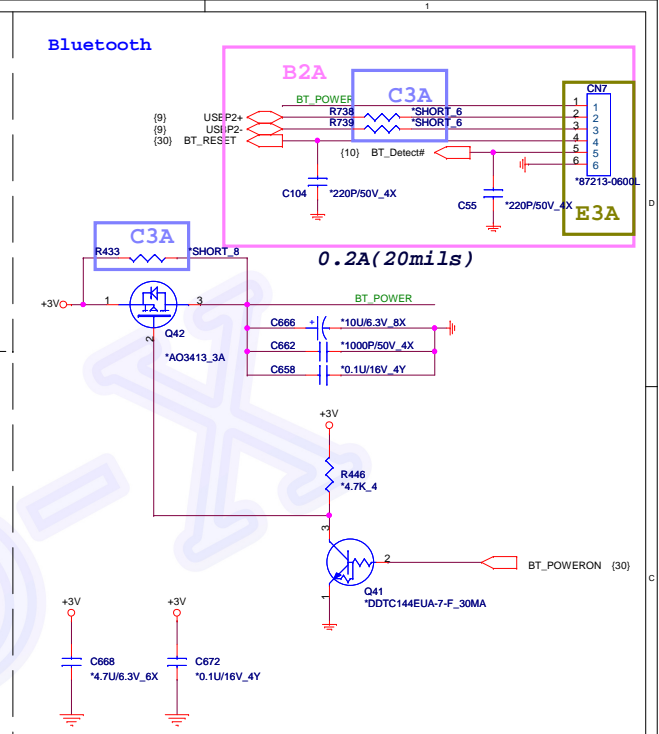
Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET



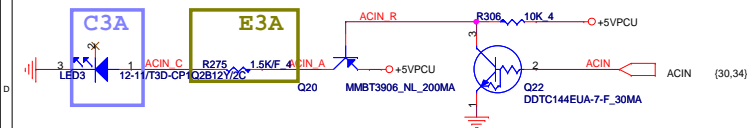
HWPG



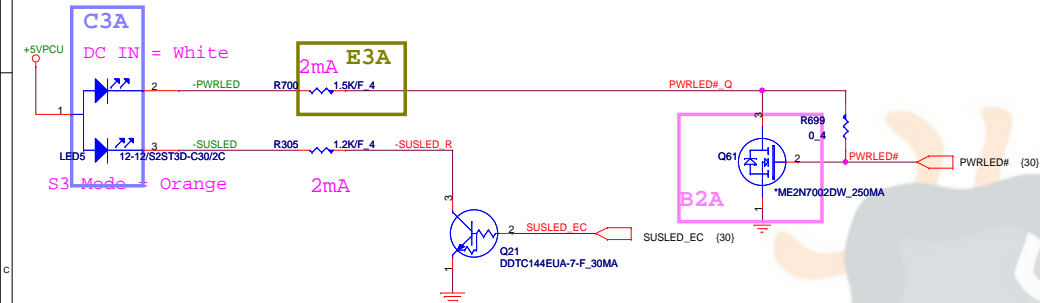


LED

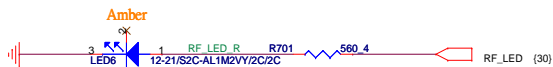
AC-IN



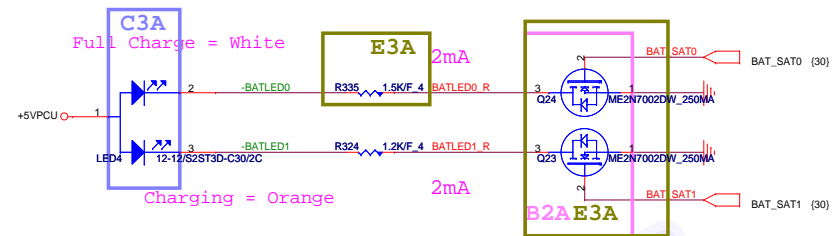
POWER



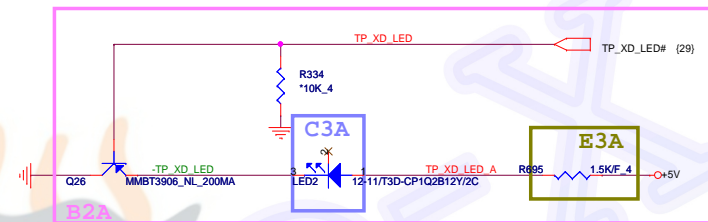
RF LED



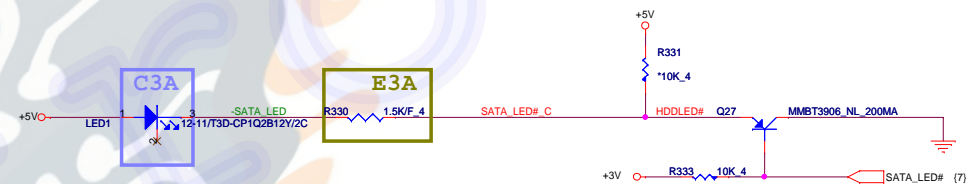
BATTERY



CARDREADER

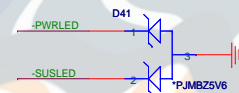


HDD/ODD

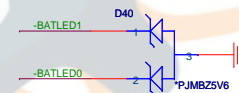


ESD Protect

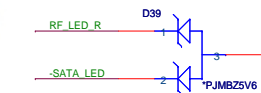
FOR POWER LED



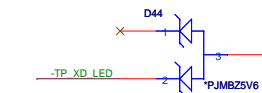
FOR BATTERY LED



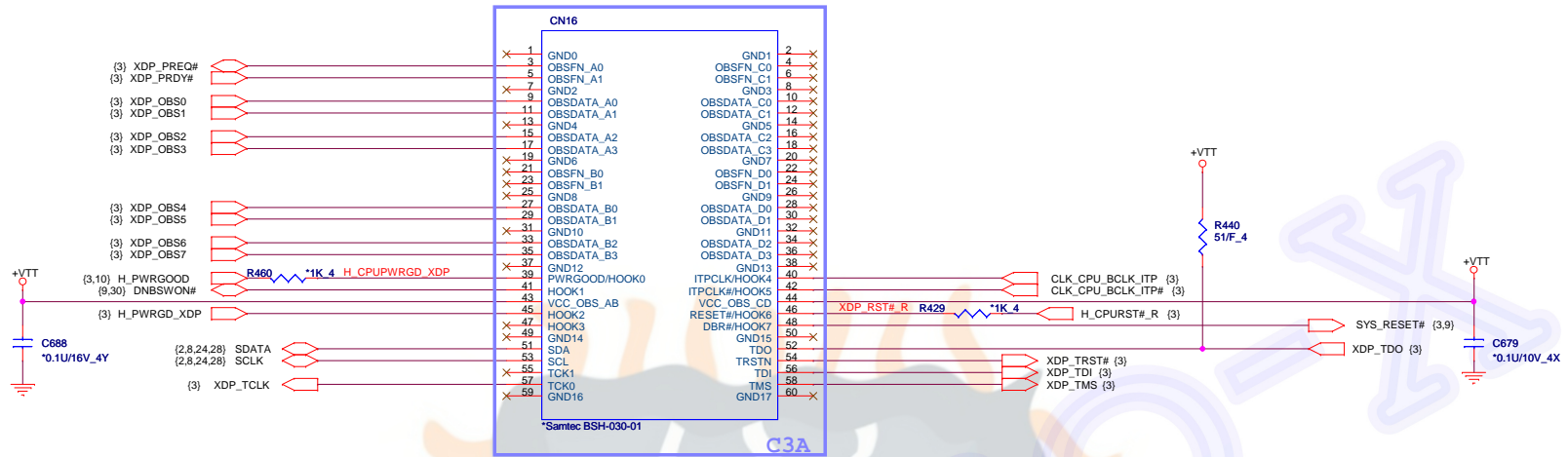
FOR HDD/RF LED



FOR CARDREADER LED



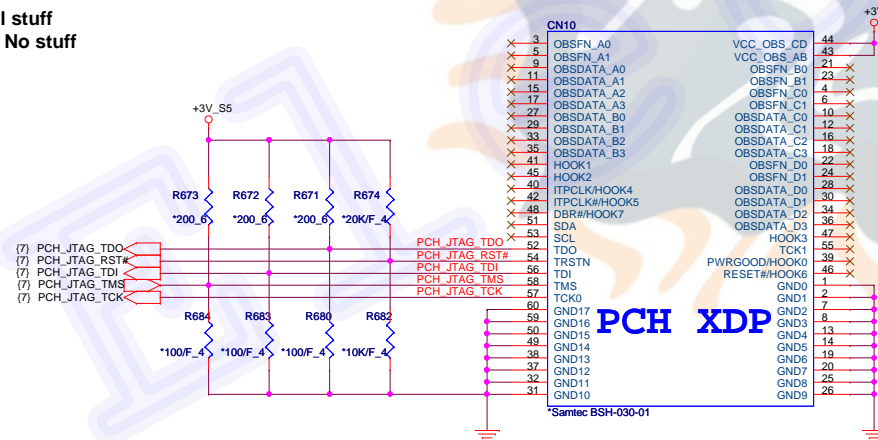
CPU XDP

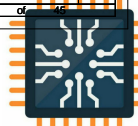
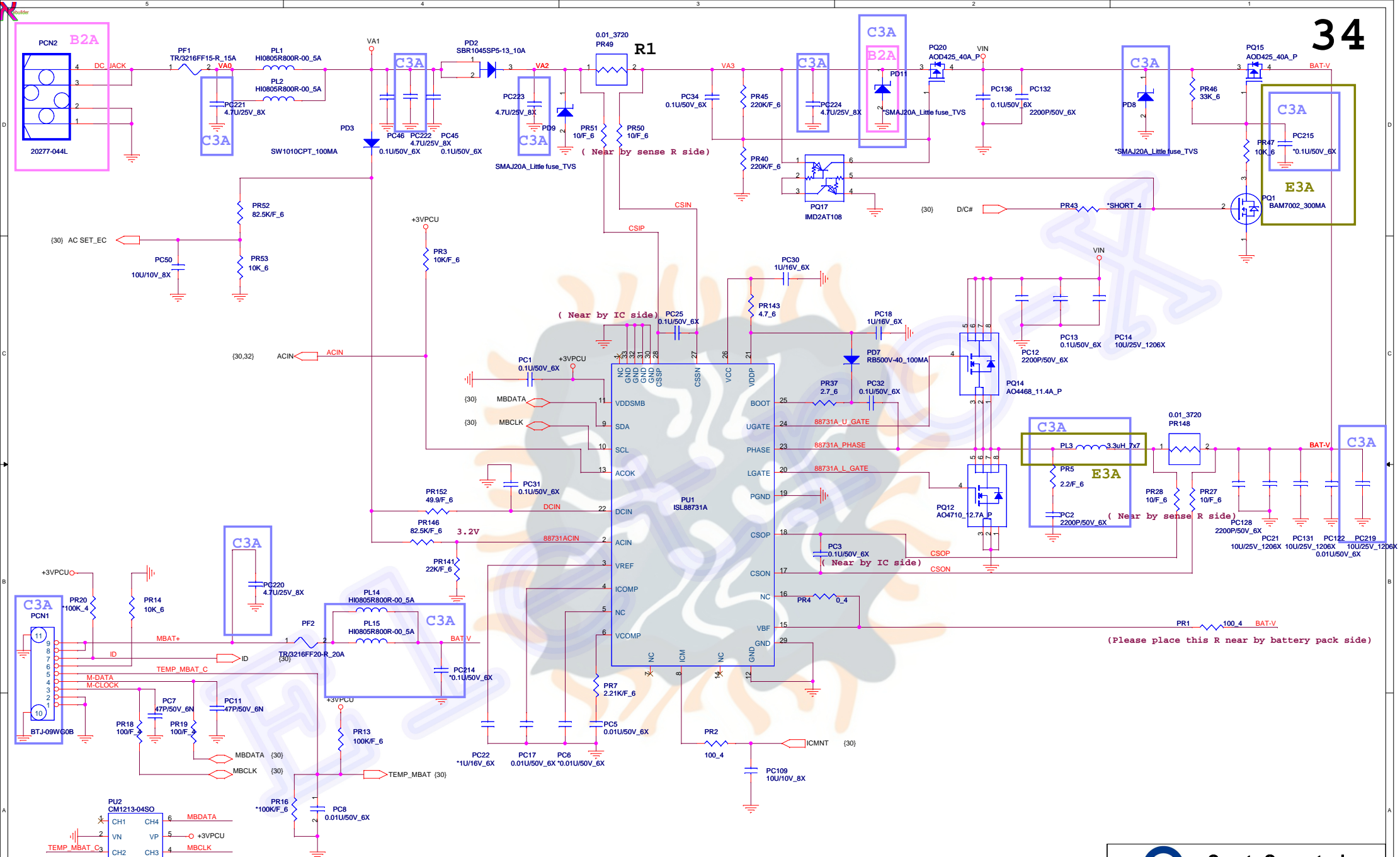


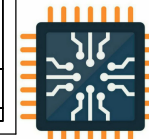
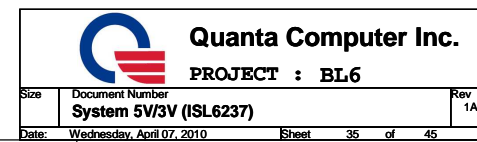
Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

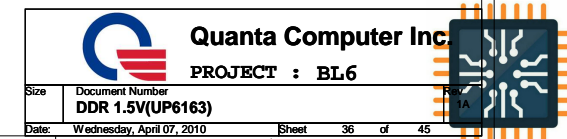
PCH XDP

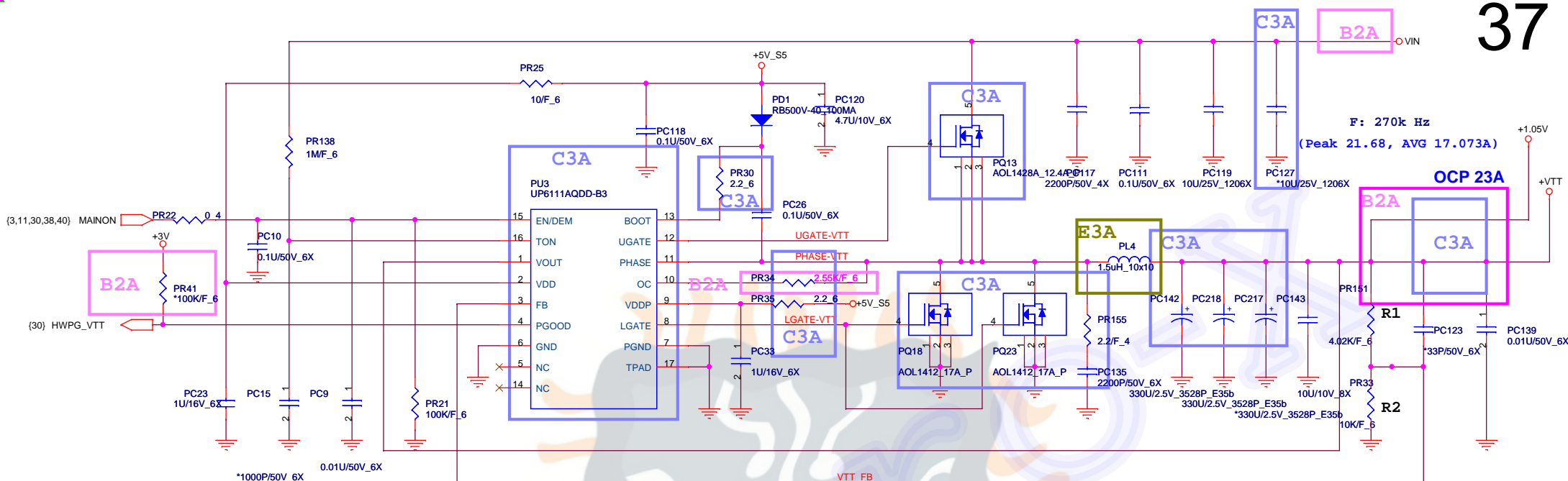
Note: For ES1/ES2 version all stuff
Production version all No stuff










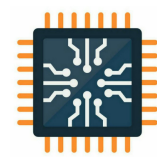


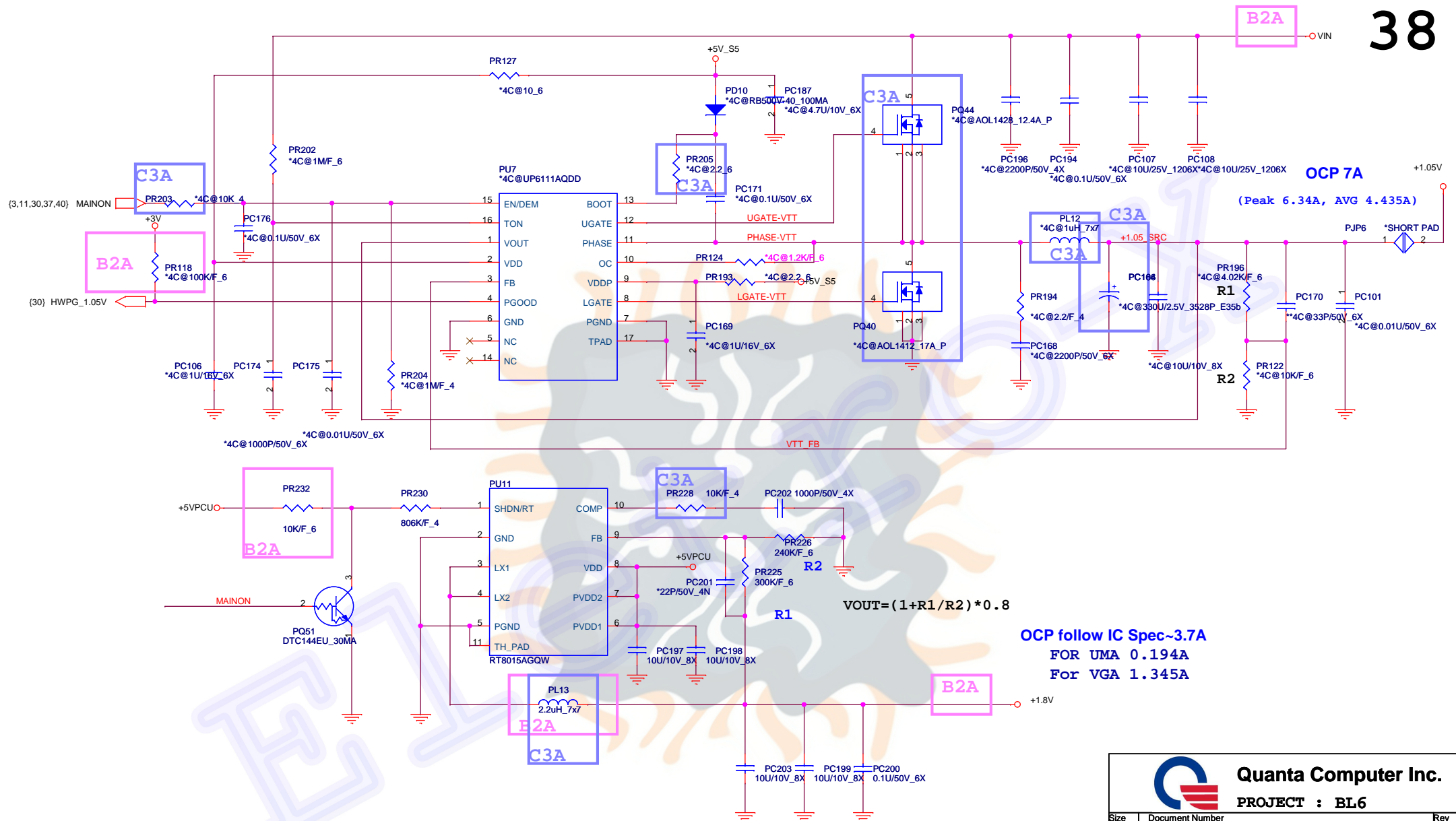
$$VOUT = (1 + R1/R2) * 0.75$$



Quanta Computer Inc.
PROJECT : BL6

Size	Document Number +VTT (UP6111A)	Rev 1A
Date:	Wednesday, April 07, 2010	Sheet 37 of 45





Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	+1.8V (RT8253)	1A
Date:	Wednesday, April 07, 2010	Sheet 38 of 45

